Overcoming Density and Power Barriers in Advanced Node SRAMs

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RAAAM™
Memory Technologies

On-Chip Memory Dictates the Cost of Digital Chips

- On-Chip **memory dominates** the **chip area / cost** of all digital applications
- On-Chip **memory capacities** follow ever **increasing** data demands
- **Insufficient** on-chip **memory** leads to **extreme power consumption** under AI workload

AI & Datacenter

On-Chip Memory Area >60%

NVIDIA — A100 7nm

Mobile

On-Chip Memory Area >45%

A14 5nm

Automotive

On-Chip Memory Area >35%

TESLA — FSD 14nm

AI Training

On-Chip Memory Area >25%

cerebras — WSE 5nm

* Examples of Chips and On-Chip Memory Area [%] Across Different Digital Applications

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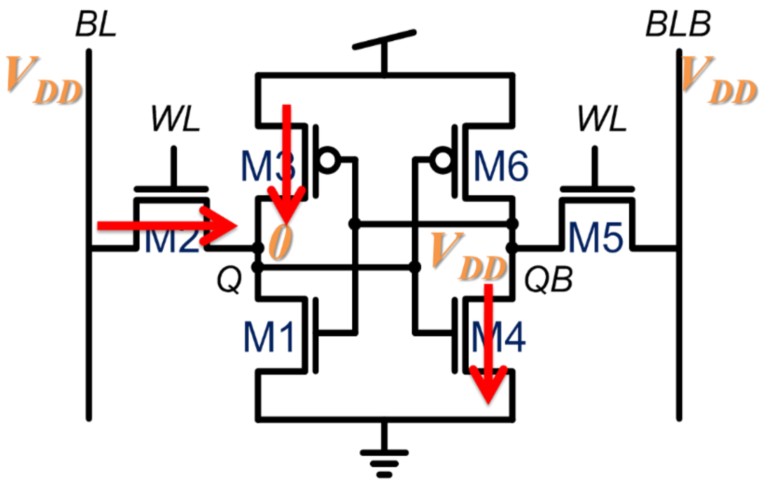
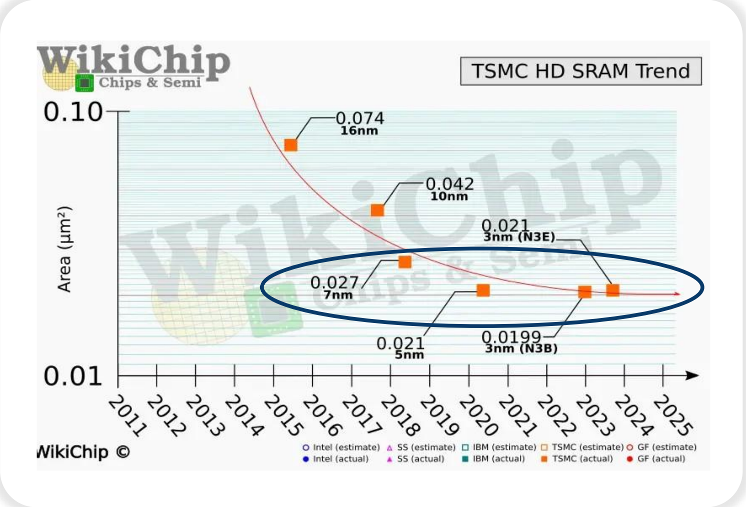
Problem: SRAM Scaling Has Ended

6T SRAM Schematic



- **Ratioed Bitcell** Limits Yield
- Multiple Failure Mechanisms
- Multiple Leakage Paths
- Single-Ported

Reported HD SRAM Cell



- DTCO not effective for SRAM beyond 10nm
- Effectiveness of SRAM Scaling Reduces
- Memory Bottleneck Increases

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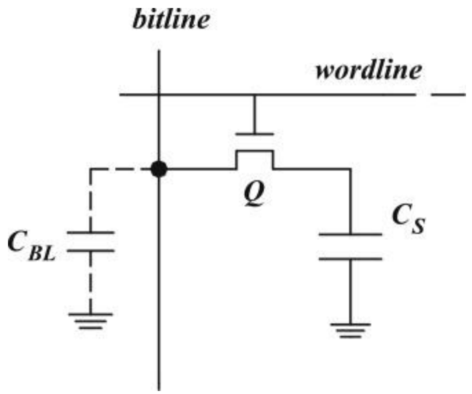
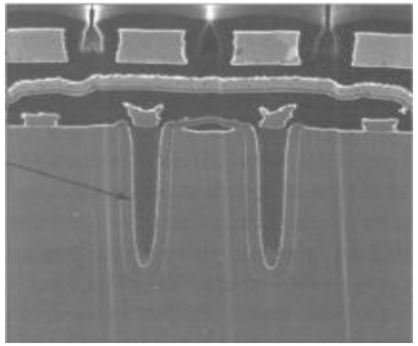
1T-1C Embedded DRAM

- 1T-1C eDRAM offers >2X higher density than 6T SRAM

BUT:

- Requires fabrication of a large SN capacitor (few pF)
  - Readout depends on charge sharing between Cbl and Cs
- **Additional process steps and cost** (trench caps)
- **Reliability issues** in scaled technologies due to readout relying on charge sharing
  - Significant capacitance decrease to ~10fF (14nm, IBM)
- And more (destructive read, special thick gate oxide, multiple assist voltages)





Trench cap

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RAAAM's GCRAM Overcomes SRAM and 1T1C eDRAM Limitations

- **Extending the scaling** of on-chip memories
- Up-to **50% area reduction** vs. SRAM
- Up-to **10X power reduction** vs. SRAM
- **Standard CMOS** process – **no additional** masks or **cost**
- **Active read port – no charge sharing or write back necessary**
- **15 Test-Chips at leading foundries down-to TSMC N5, N2 in development**

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RAAAM's GCRAM Follows Over 10 Years of R&D and 22 Patents

SRAM Bitcell

6/8 Transistors per bit of data

Innovation

Bitcell Size Reduction

GCRAM Bitcell

3 Transistors per bit of data

The memory area is proportional to the number of bitcell transistors

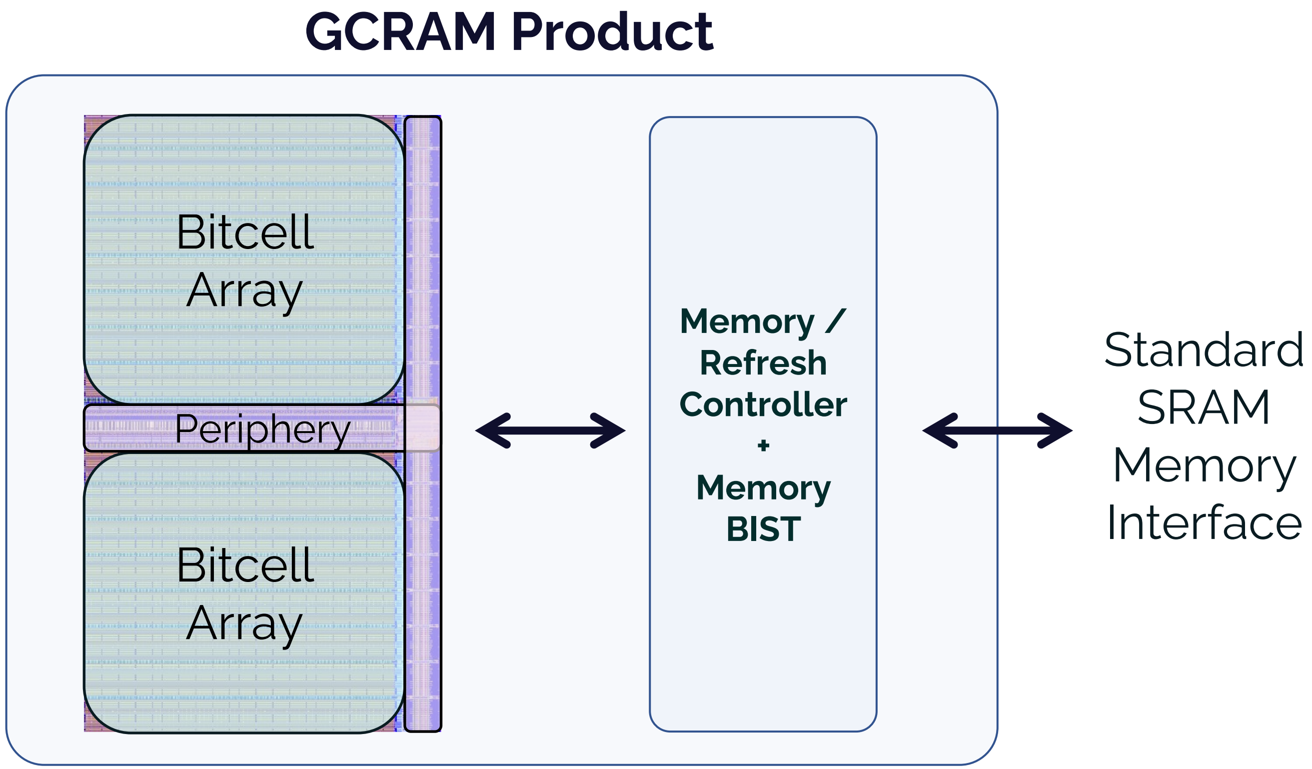
GCRAM Technology Developments

Memory Controller	• Refresh Algorithms for 100% Availability. • Support in Standard SRAM Interface.
Architecture and Periphery	• Word-Line Assist • PVT-compensating reference generation • Offset-cancelling Sense Amplifier • Refresh process monitors
Bitcell Array	• Ultra High-Density Layout • Low Leakage Bitcell Design

Memory Technologies

GCRAM Product Offers a Drop-In SRAM Replacement

- Standard SRAM Interface
- Two-ported operation
- Single-cycle write and read
- Non-destructive read operation
- Single-cycle refresh
- Compiler support for up-to 1024bit I/O and multi-Mbit instances



Technology Status

- Silicon validated and fully characterized in TSMC N16, N5
- Customer silicon validated on TSMC N16, N5 in progress
- Development at **TSMC N2**, first test-chip tapeouts w. customers in H1/26
- Full **N2 qualification in H1/27**
- Development at **GlobalFoundries 22FDX**, Q1/26 tapeout, **H1/27 qualification**

Thank You!

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