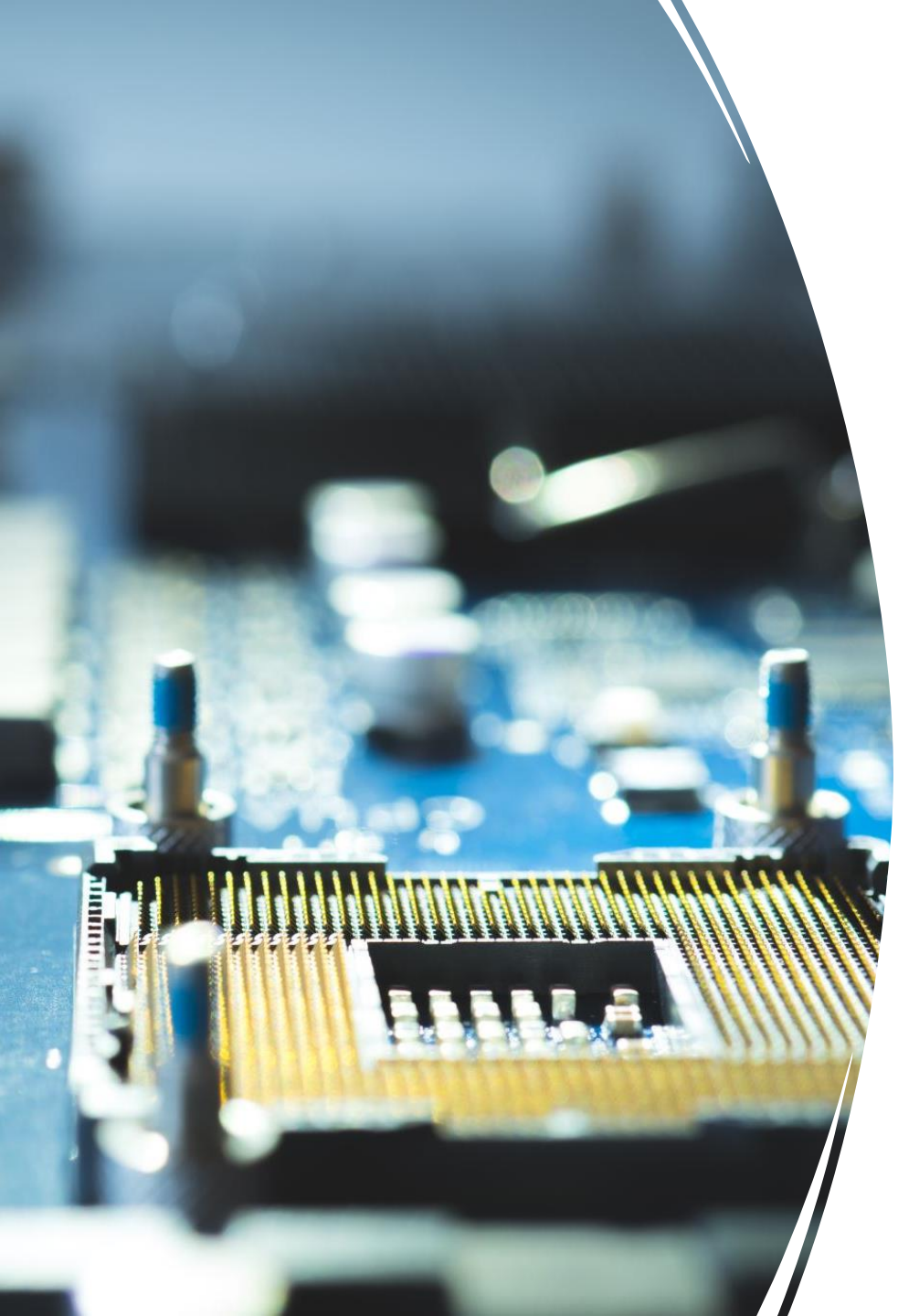


Is RTL Holding Back AI Hardware Generation?

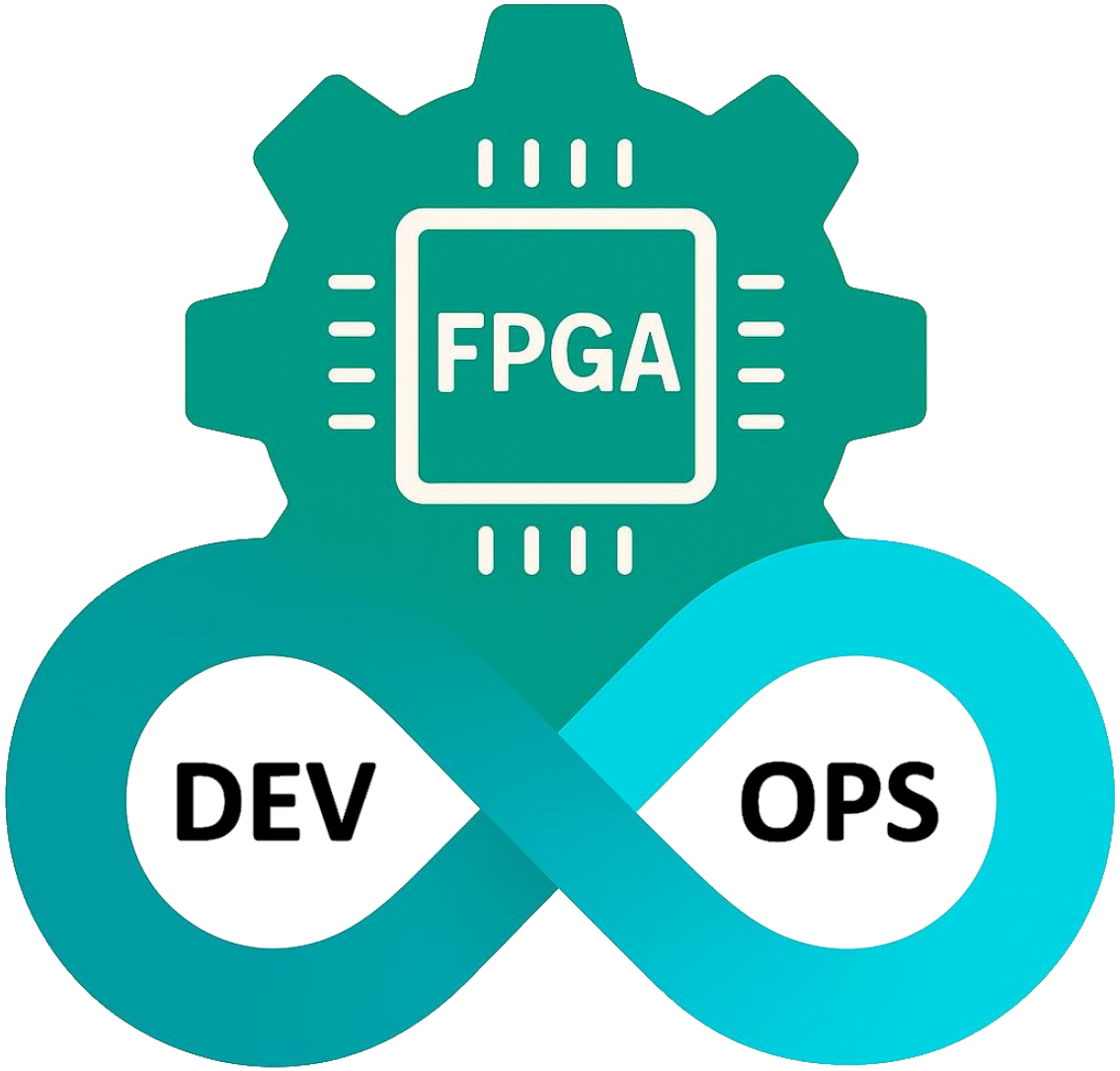
Oron Port, PhD

CEO and Cofounder

DFiant

About DFiant

www.dfiant.works



Hypothetical AI Hardware Generation Choice

A

Prompt to GDS

@ 99% Success

B

Prompt to Verilog

@ 80% Success

$$t_{A@100\%} \gg t_{B@100\%}$$

Hypothetical AI Hardware Generation Choice

A

Prompt to GDS
@ 99% Success

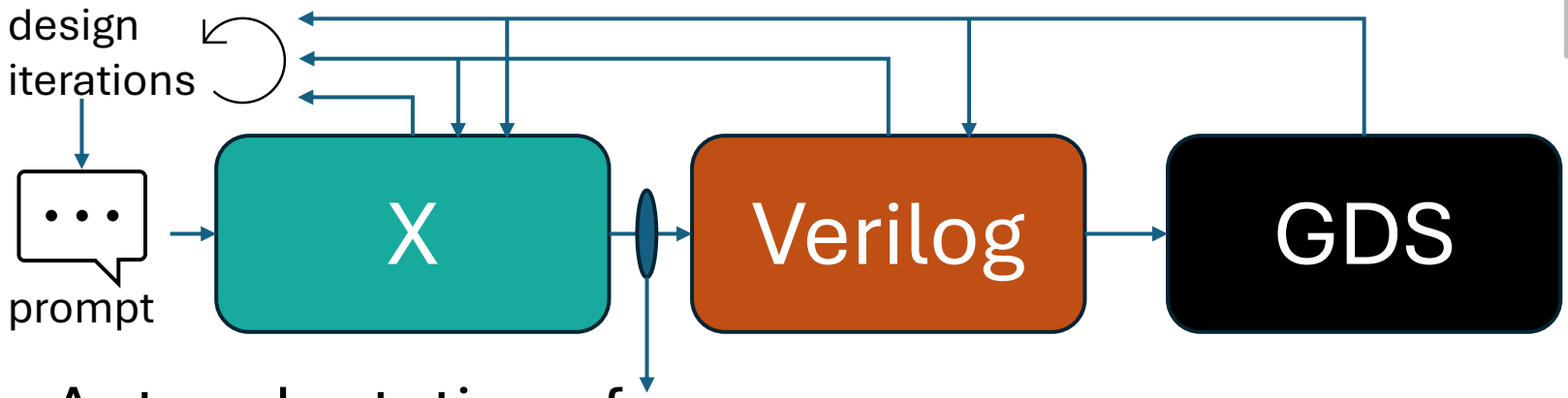
B

Prompt to Verilog
@ 80% Success

C

Prompt to X
@ Y% Success

$$t_{A@100\%} \gg t_{B@100\%} \gg t_{C@100\%}$$



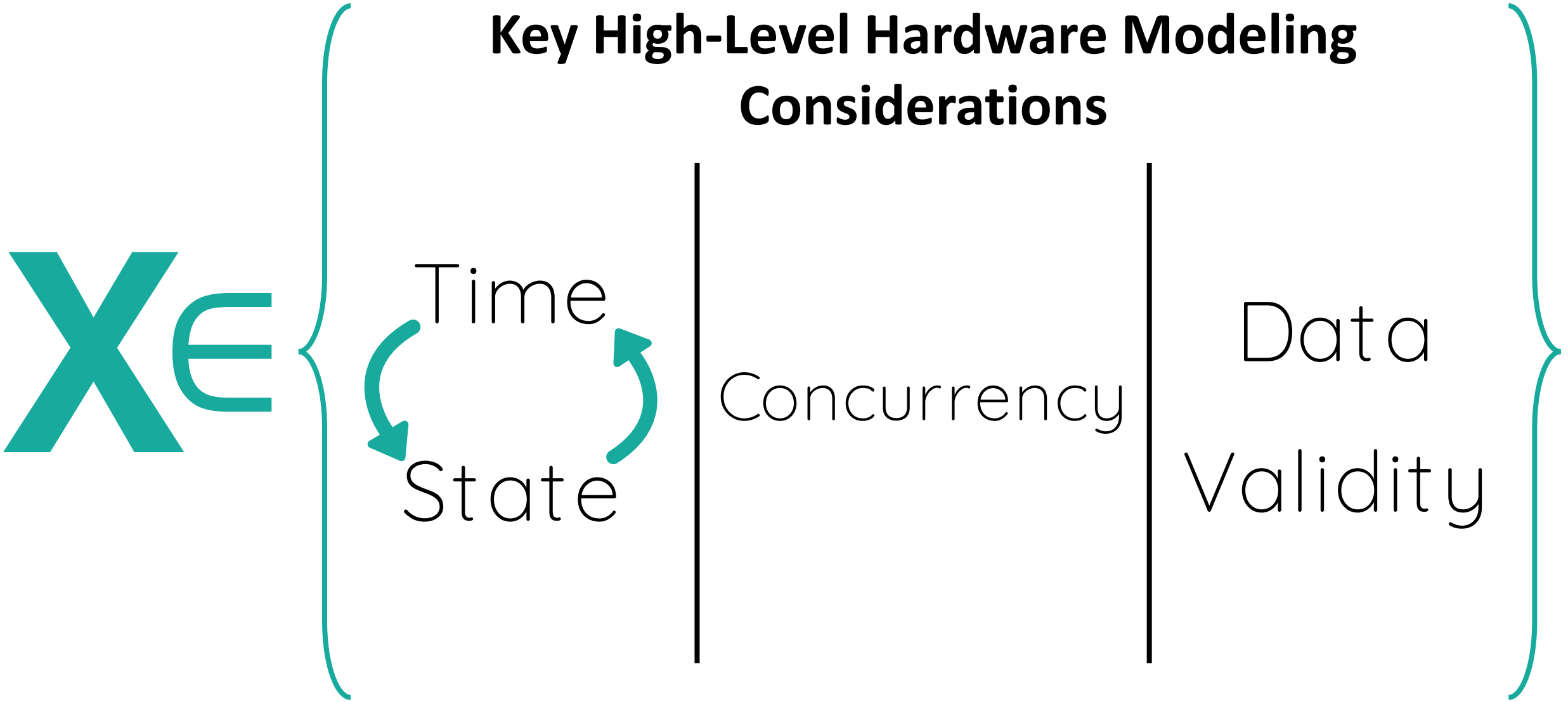
Auto adaptations for:

- (Functional) Simulation Speedup
- Design Metric Optimizations:
  - Performance
  - Latency
  - Power
- Design Partitioning:
  - Embedding FPGA Cores
  - Emulation and Prototyping
  - Monolithic to Chiplets

Truly Agnostic
Hardware Description Language

Meaning, ***not HLS nor RTL***

Key High-Level Hardware Modeling Considerations



HDL Alternatives

DFiant

Independent

Unique syntax	Inspired	
Silice	Spade	*by Rust*
Veryl	TL-Verilog	*by Verilog*
SUS	VHDP	*by VHDL*
BSV	PipelineC	*by C*

Dependent

Clash 

MyHDL, CoHDL 

Hosted DSLs

DFHDL, Chisel, SpinalHDL 

Migen, Amaranth 

RustHDL, RHDL 

ROHD 

Hardcaml 

QuSoC 

https://tinyurl.com/hdl-list by Frans Skarman

DFHDL Design Domains

XX	Abstraction	Correctness	Synthesizability	Simulation
DF	Dataflow	Guaranteed ✓	Guaranteed ✓	Functional
RT	Register Transfer	Unknown ?	Guaranteed ✓	Cycle Accurate
ED	Event Driven	Unknown ?	Unknown ?	Event Based

```
class __design_name__ extends XXDesign:
```

- **Claim**: “But everyone uses Verilog…”
- **Reality**: Many use custom HDLs or additional scripting to deal with Verilog’s shortcomings

- **Claim**: “Alternative HDLs used only in Academia”
- **Reality**: Chisel-based design power SiFive IPs and several others too. SpinalHDL FPGA design worked in Space

- **Claim**: “Too much legacy Verilog IP”
- **Counter-claim**: AI can be leveraged to “decompile” legacy to alternative HDLs.

Summary

https://dfianthdl.github.io

A

Prompt to GDS
@ 99% Success

B

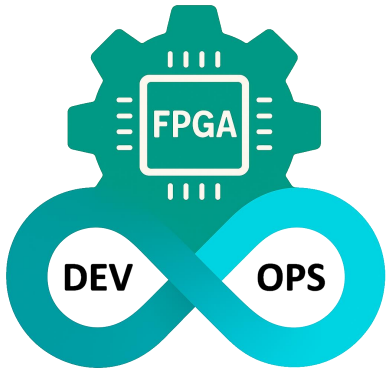
Prompt to Verilog
@ 80% Success

C

Prompt to X
@ Y% Success

$$t_{A@100\%} \gg t_{B@100\%} \gg t_{C@100\%}$$

Thank You!



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