



In-System Test, A critical element to SLM

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Agenda

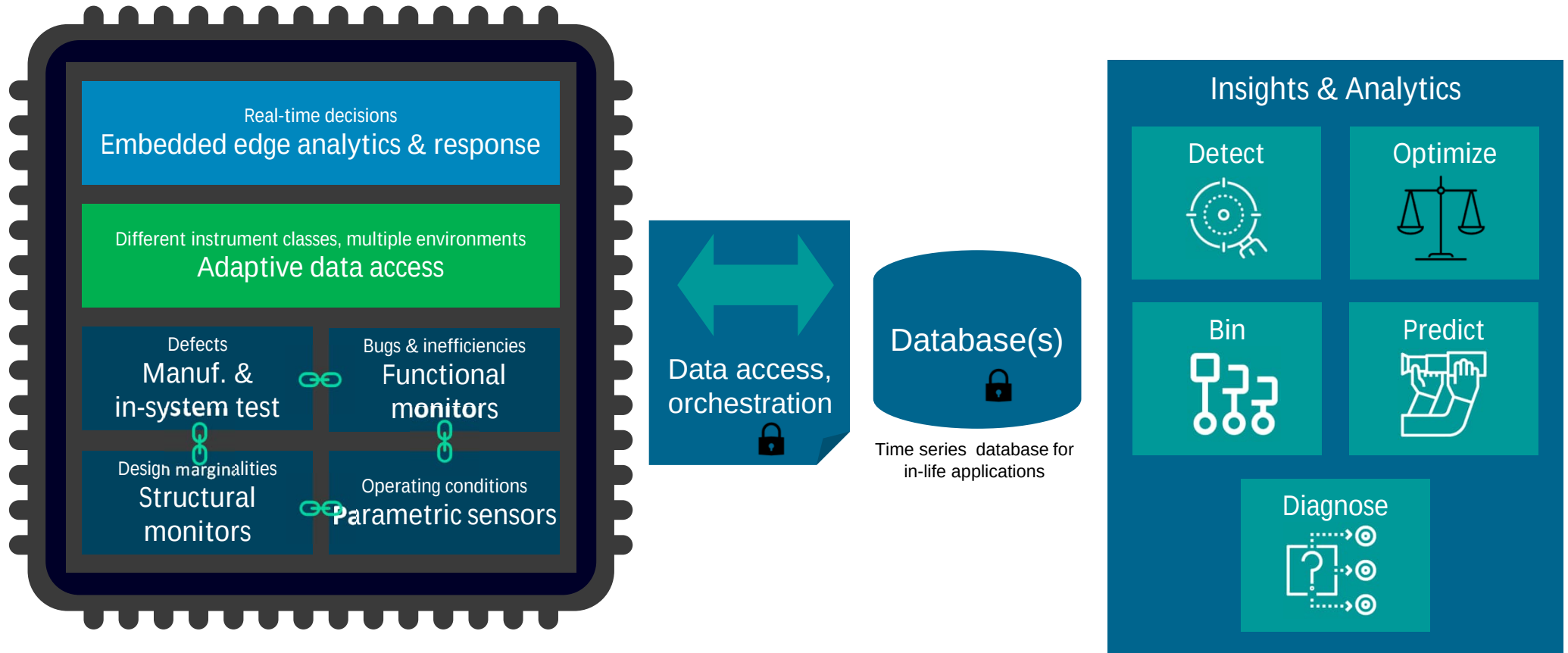
SLM and market drivers

Causes of in-field device failures

In-system testing options

Tessent solutions

Silicon Lifecycle Management



Monitoring data center health will extend their longevity

Big Tech boosts profits by \$10bn with accounting change to server life estimate

Alphabet, Amazon, Microsoft and Meta have all shifted estimates of how long they will use technical equipment

Google

Increases server life from 4 & 5 years to 6

Amazon

Extends server life from 4 years to 5

Microsoft

Extends server life from 4 years to 6

Meta

Meta reduces depreciation costs

Financial Times
Tabby Kinder and Camilla Hodgson in San Francisco and Cristina Criddle in London, February 4 2024

Data Center Silent Data Errors: Implications to Artificial Intelligence Workloads & Mitigations

B. Bittel, M. Shamsa, B. Inkley, A. Gur, D. Lerner, and M. Adams

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Cores that don't count

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Silent Data Corruptions at Scale

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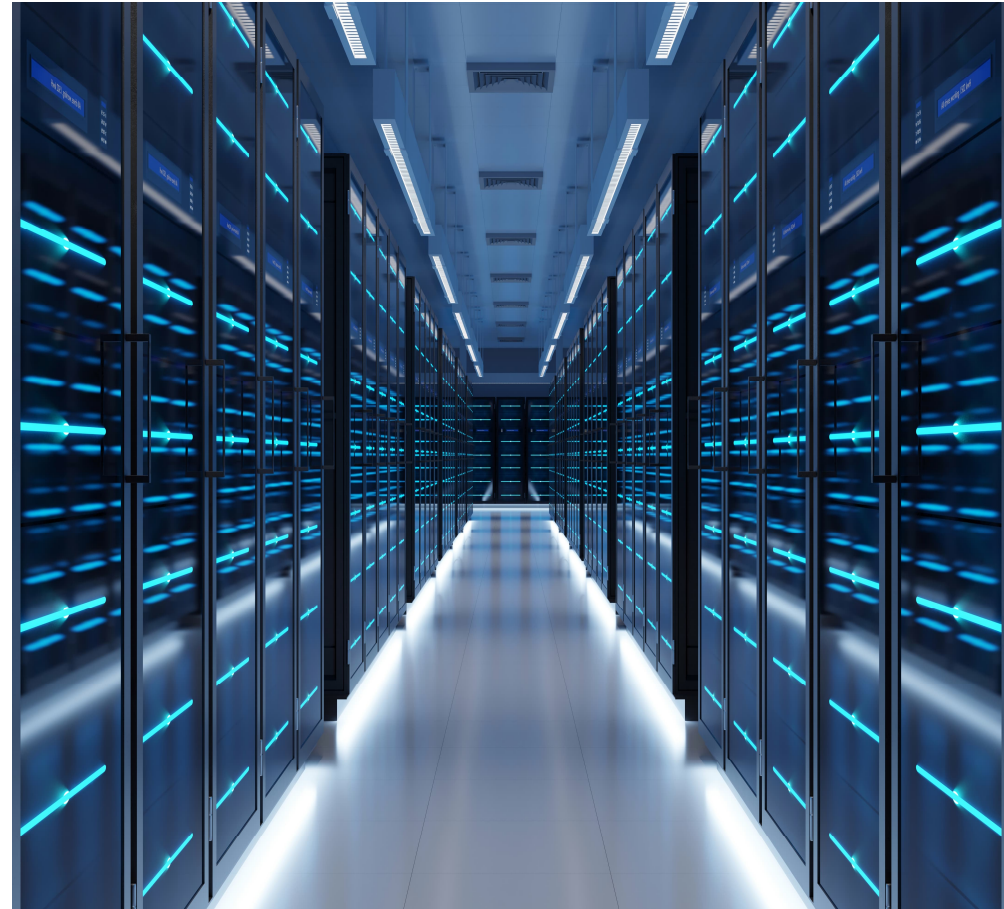
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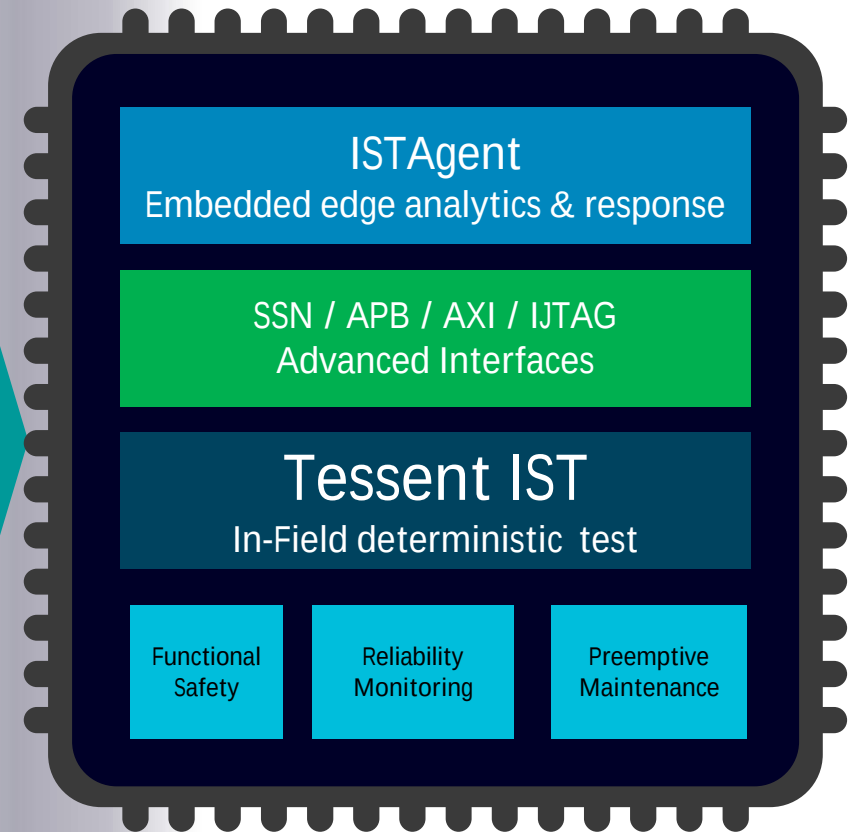
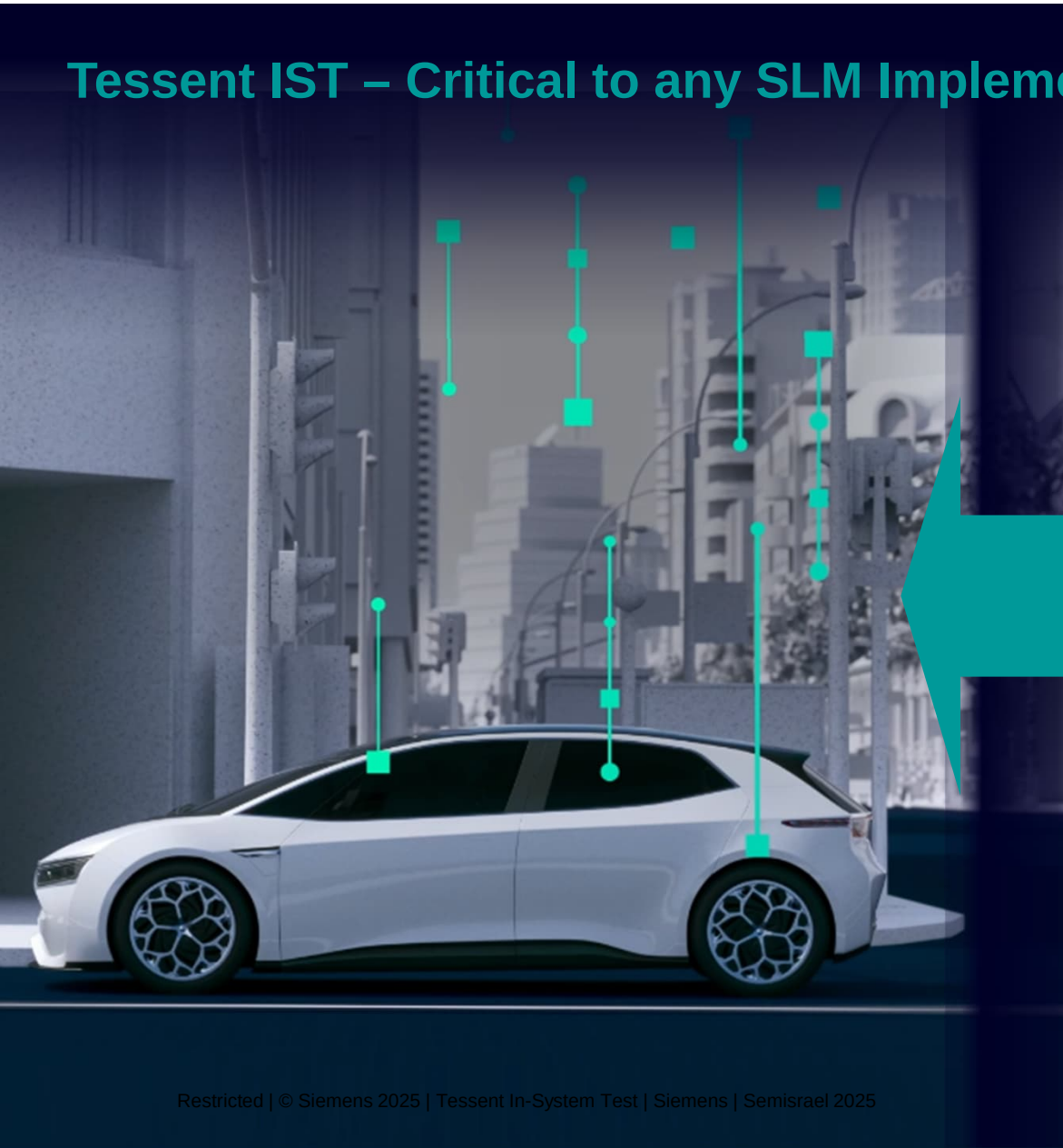
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High reliability, zero down time applications

- Manufacturing quality testing capability
- Flexibility to have updatable pattern content to aid silicon lifecycle management
- Capability to add new tests to address SDE
- Run as part of a periodic maintenance schedule
- Full diagnostics capability available

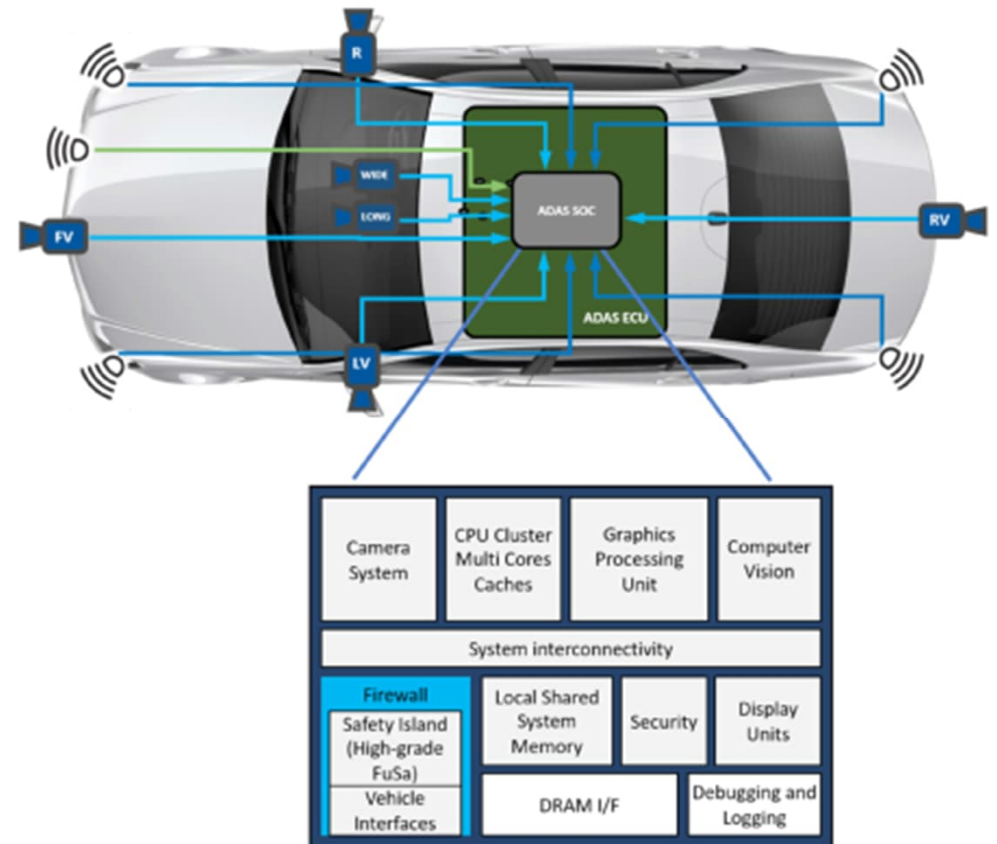


Tessent IST – Critical to any SLM Implementation



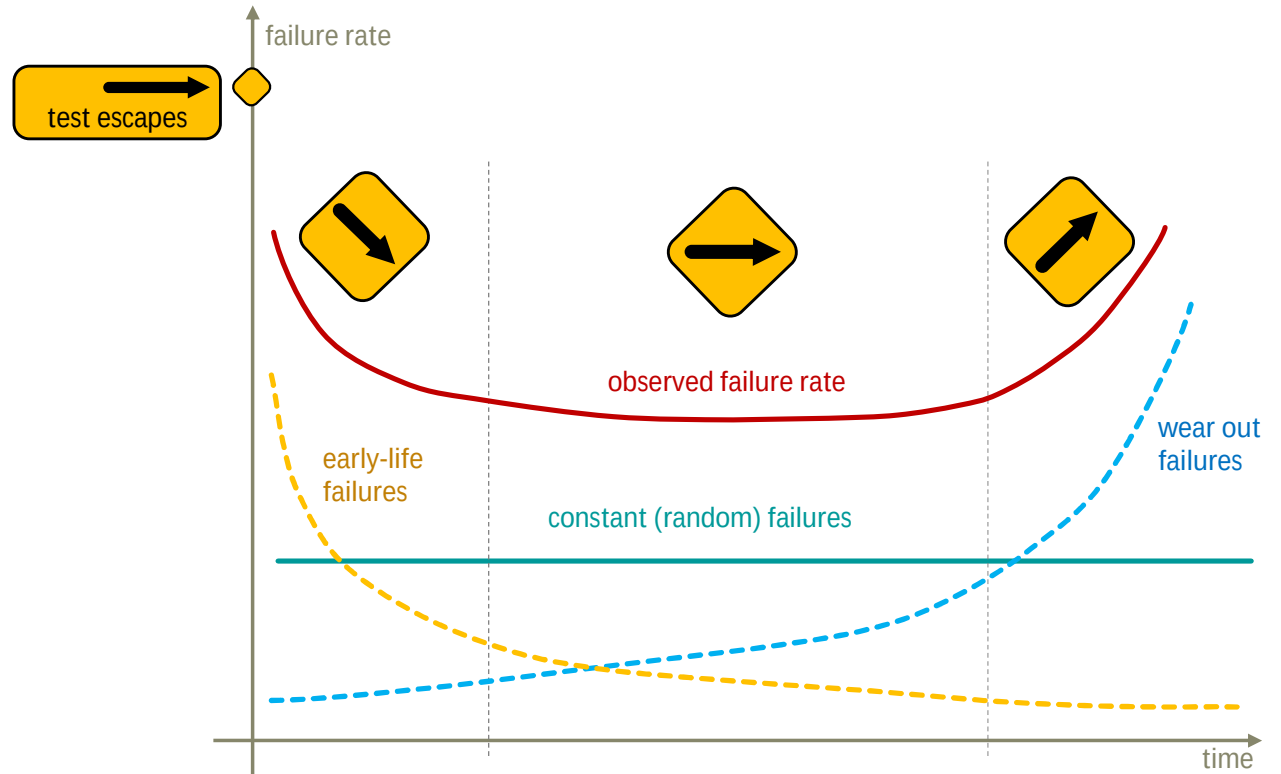
Safety and security focused applications

- Safety mechanism for functional safety application required
- Capability to run Key-on / Key-off or Periodic
- High speed to meet FTTI requirement
- High coverage to meet and exceed ISO26262 requirements
- Flexibility to have updatable pattern content to aid silicon lifecycle management



Why is in-system testing required?

- Subtle defects
- Small delay faults
- Test escapes caused by test marginalities
- Early-life failures
- Random failures
- Aging
- Incomplete coverage

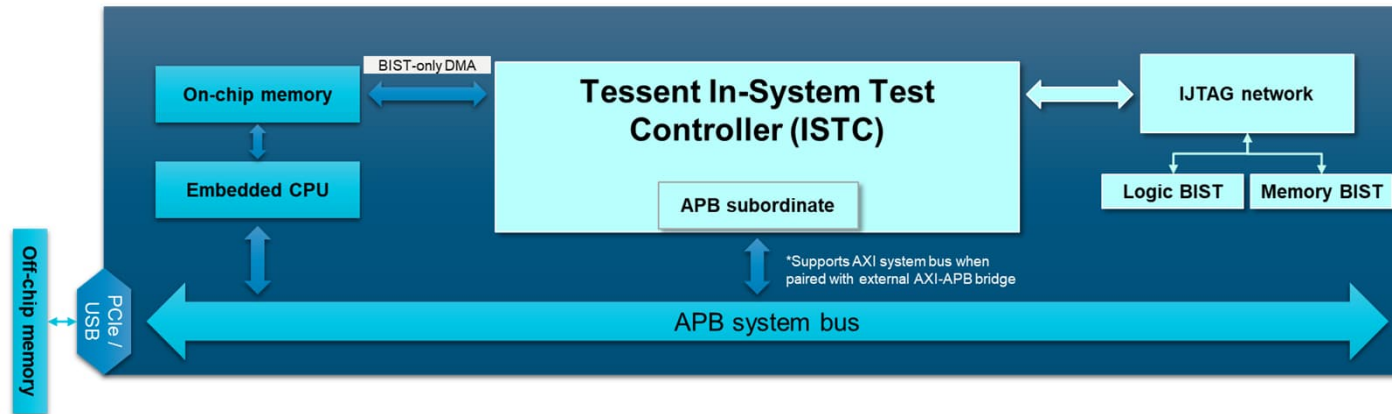


Choosing deterministic test vs. logic BIST

Requirements		Pseudo-random tests (LogicBIST)	Deterministic tests (FastScan / TestKompress)
Test quality	High test coverage, target advanced fault models including defect-aware test	✓	✓✓✓
Test time	Ability to achieve test coverage goals within a small test window	✓✓	✓✓✓
Test content	Ability to change the test content through the silicon life cycle	✓	✓✓✓
Design flow	Difficulty in implementing DFT	✓	✓✓✓
Test storage	Amount of memory needed to store test data on-chip or in-system (Memory footprint)	✓✓✓	✓

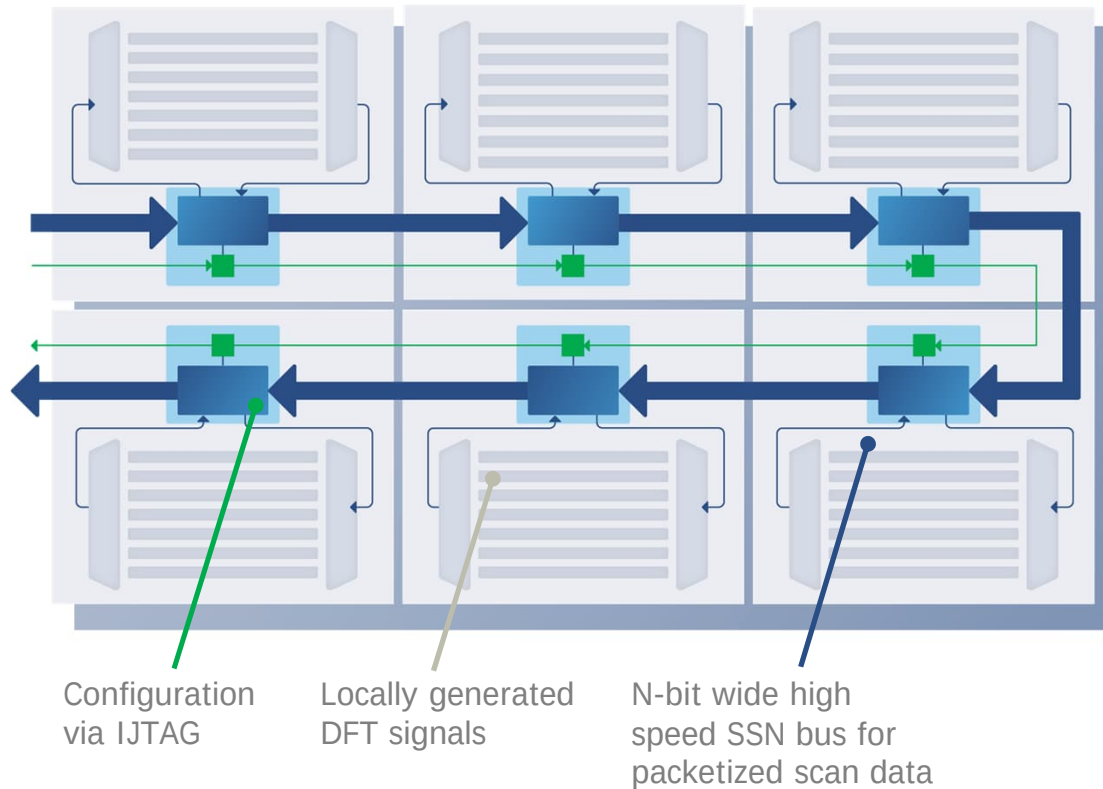
Tessent MissionMode software

Enables in-system test using BIST and IJTAG instruments



- Test data delivery through APB subordinate interface
 - Optionally, use custom direct memory access (DMA) interface for BIST tests
- Drive test execution using IJTAG network
 - Intercept and control JTAG (IEEE 1149.1) and IJTAG (IEEE 1687) networks
 - Execute logic BIST and memory BIST go/no-go tests for in-system test

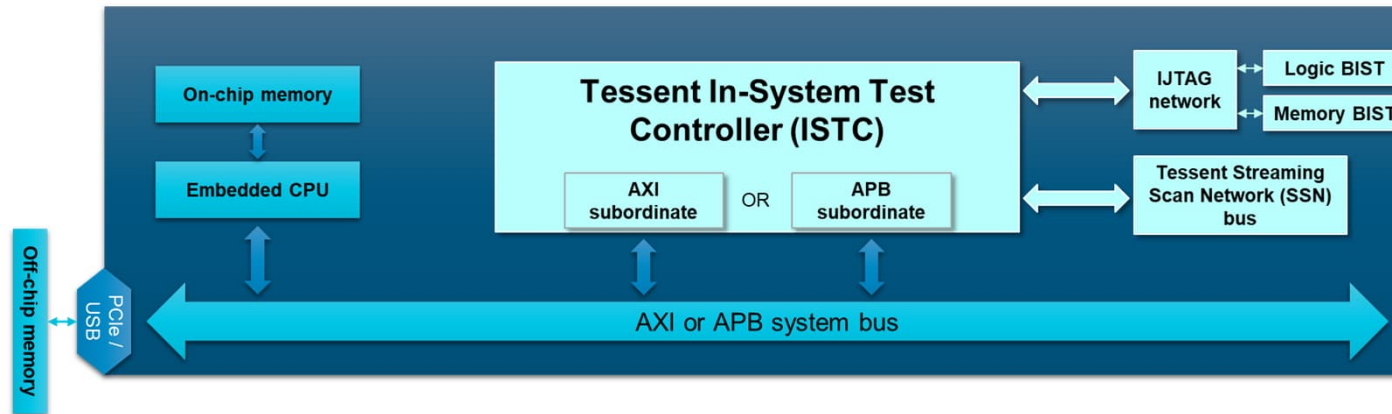
SSN - Packetized Scan Network



- Datapath is a synchronous N-bit wide bus
- Access through bus_in and bus_out ports
- A clock is the synchronous source
- SSH nodes transfer data between the datapath and the EDT / scan chains
- The datapath traverses the design hierarchy

Tessent In-System Test software

Enables in-system deterministic test with SSN

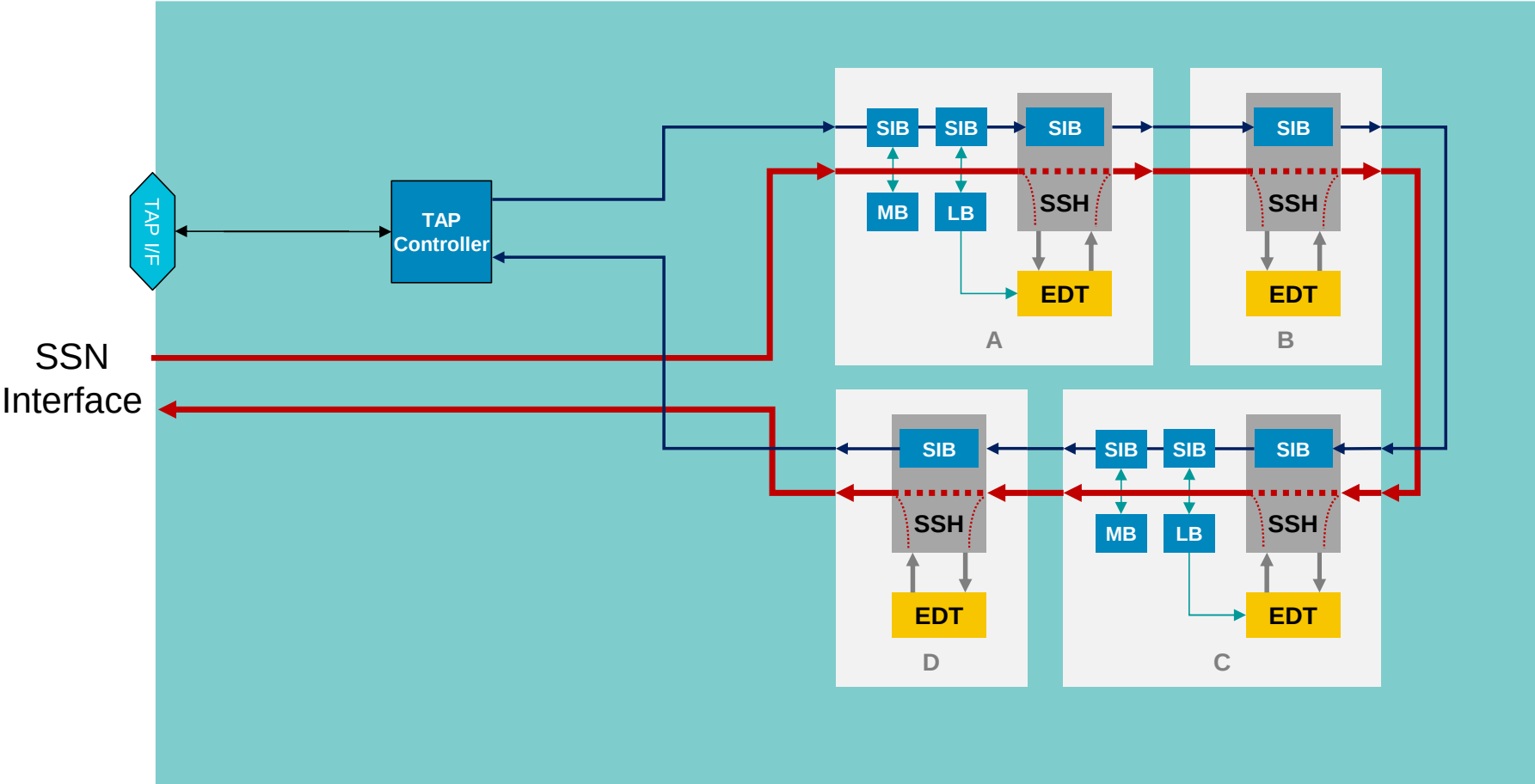


- Supports all Tessent MissionMode features for IJTAG and BIST instruments
- Supports in-system deterministic test when paired with Tessent Streaming Scan Network software
 - AXI system bus support for test data delivery
 - Improved throughput vs. test delivery over APB system bus
 - Deliver data over system bus from functional interfaces (PCIe or USB)
- Supports deterministic test delivery over the SSN bus with Tessent Streaming Scan Network
 - Target specific cell-internal and aging defects with high quality deterministic patterns
 - Change test content in-field targeting learned defectivity rates throughout silicon life cycle

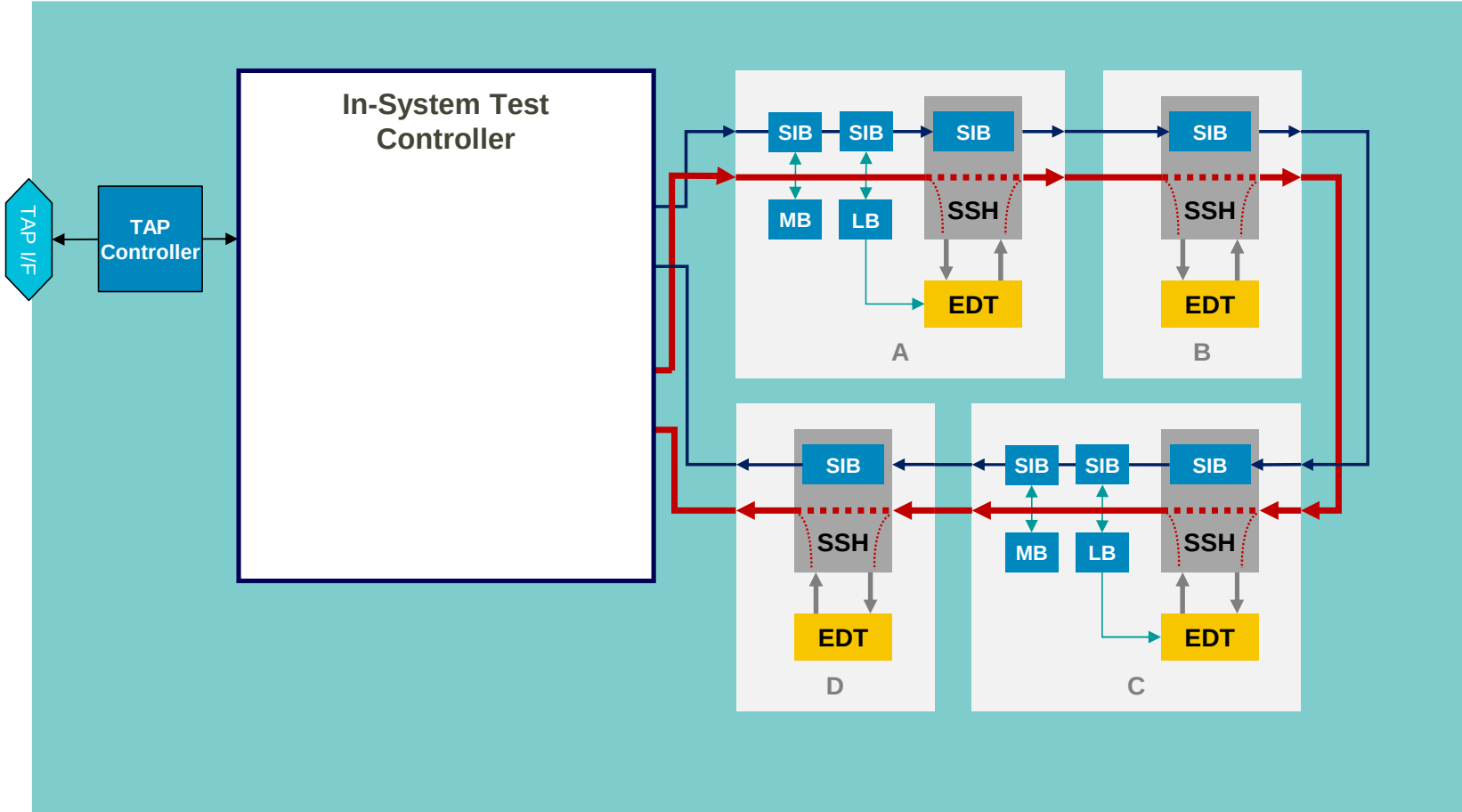
Tessent in-system test product feature comparison

Feature	Tessent MissionMode	Tessent In-System Test
Apply test data using IJTAG network	✓	✓
APB subordinate	✓	✓
BIST-only DMA	✓	✓
Apply test data using SSN network		✓
AXI subordinate		✓

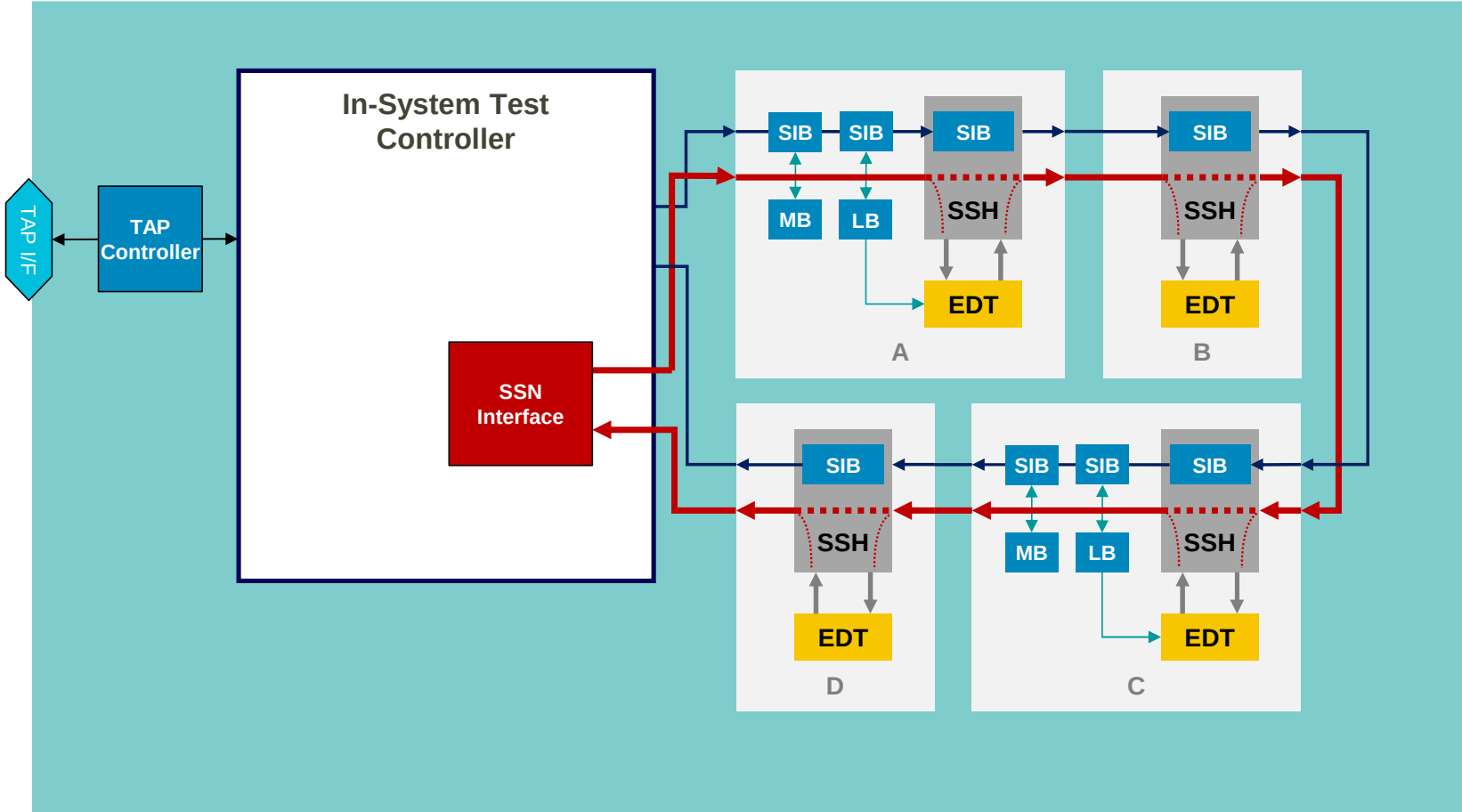
Tessent In-System Test more detailed view (1)



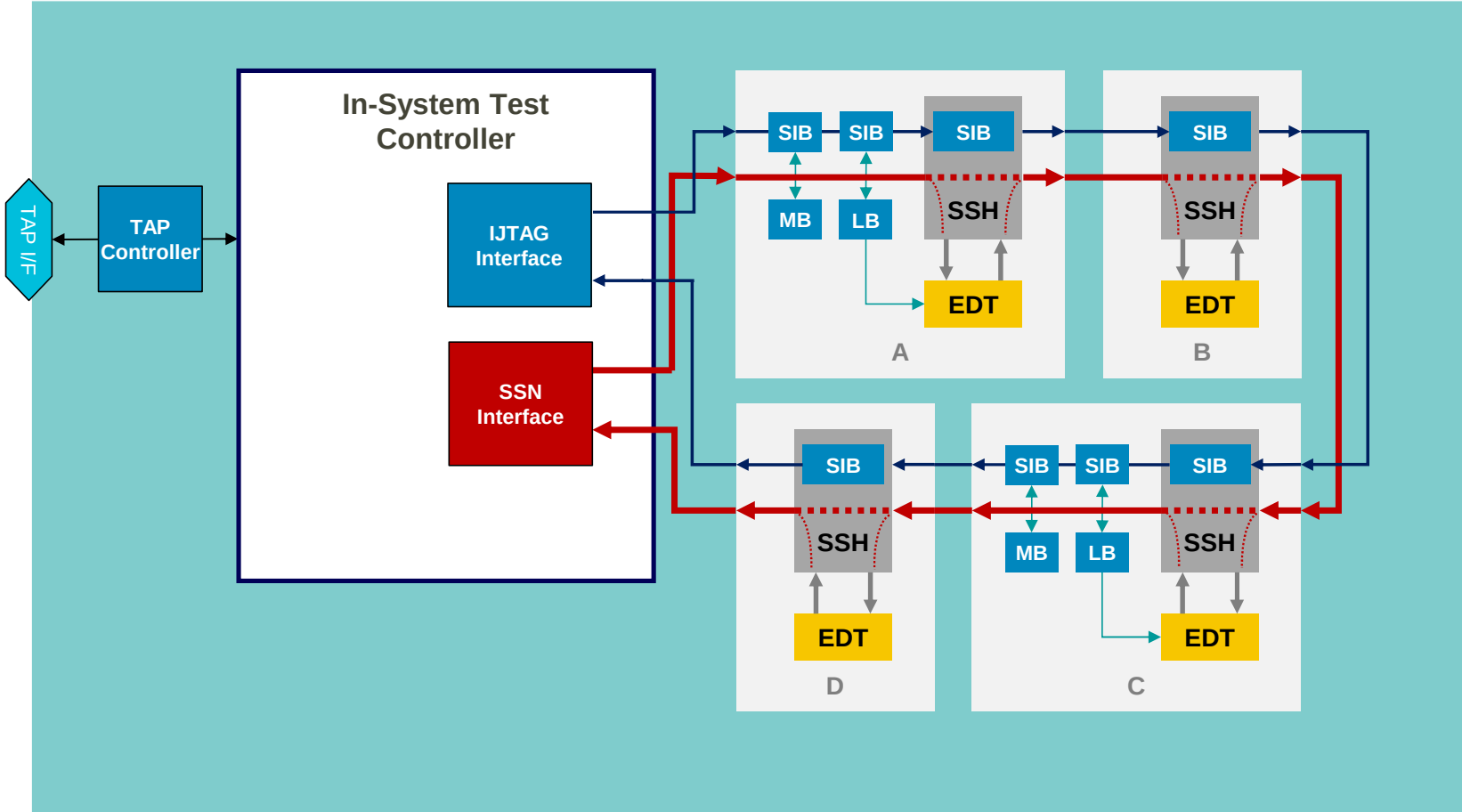
Tessent In-System Test more detailed view (2)



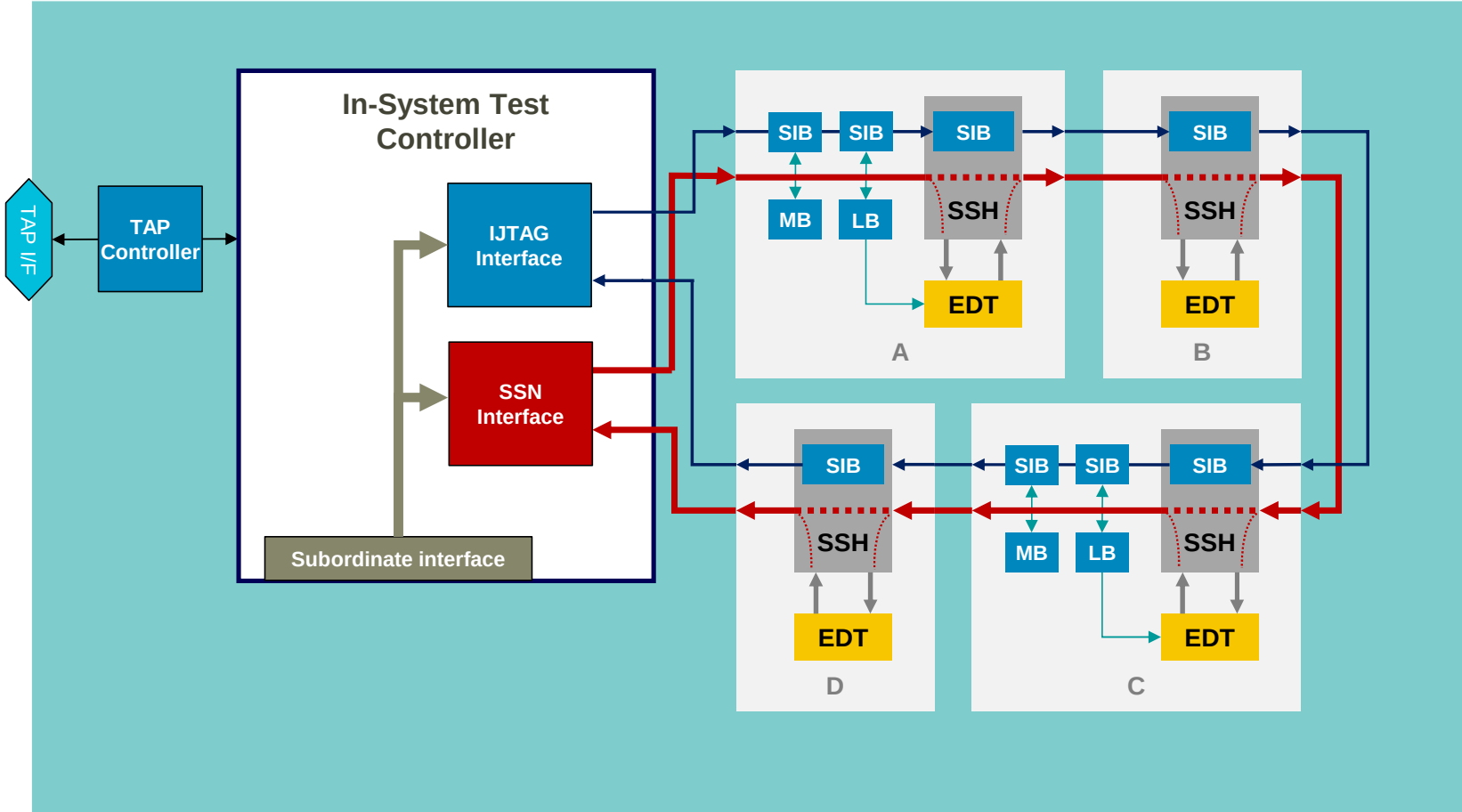
Tessent In-System Test more detailed view (3)



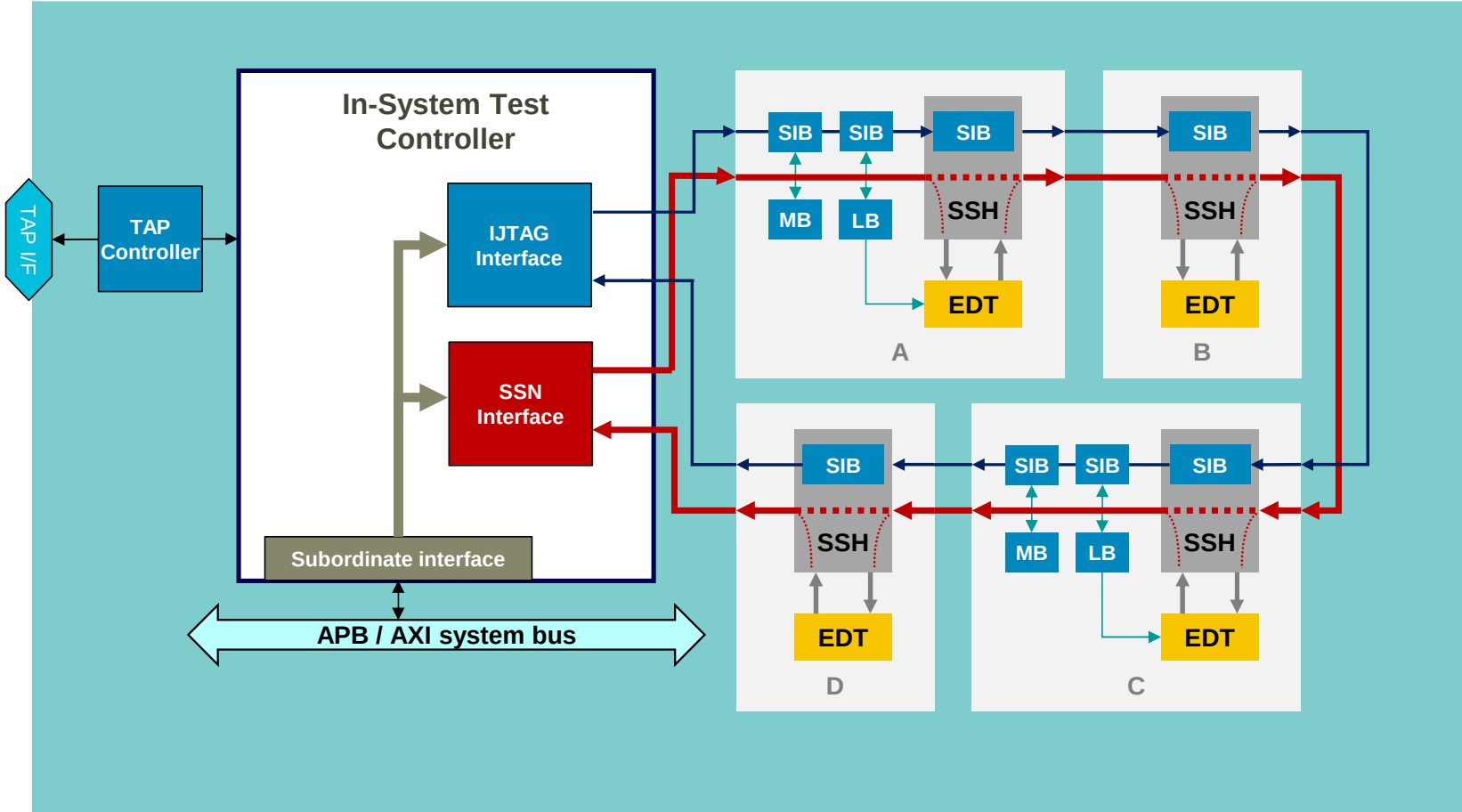
Tessent In-System Test more detailed view (4)



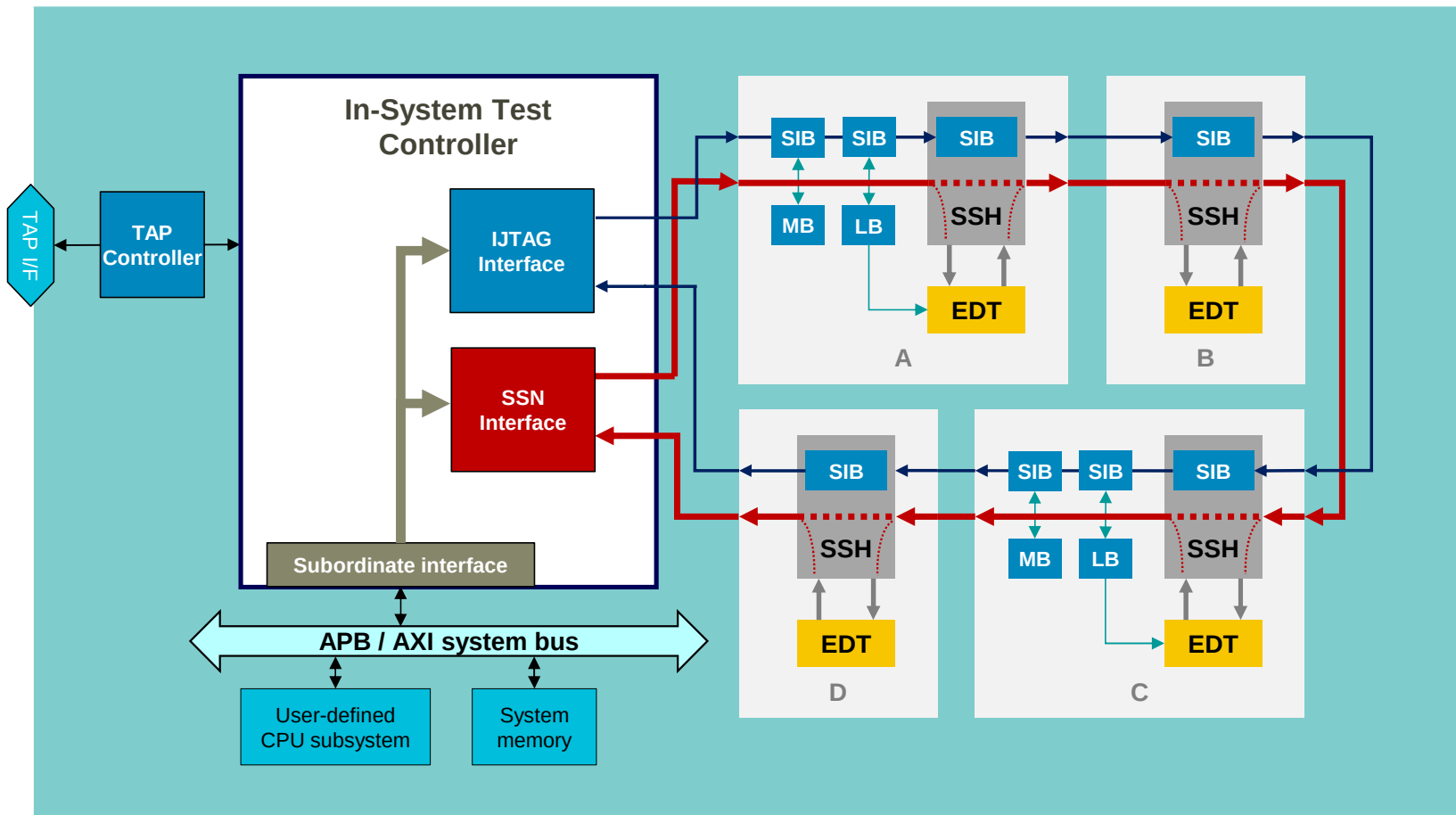
Tessent In-System Test more detailed view (5)



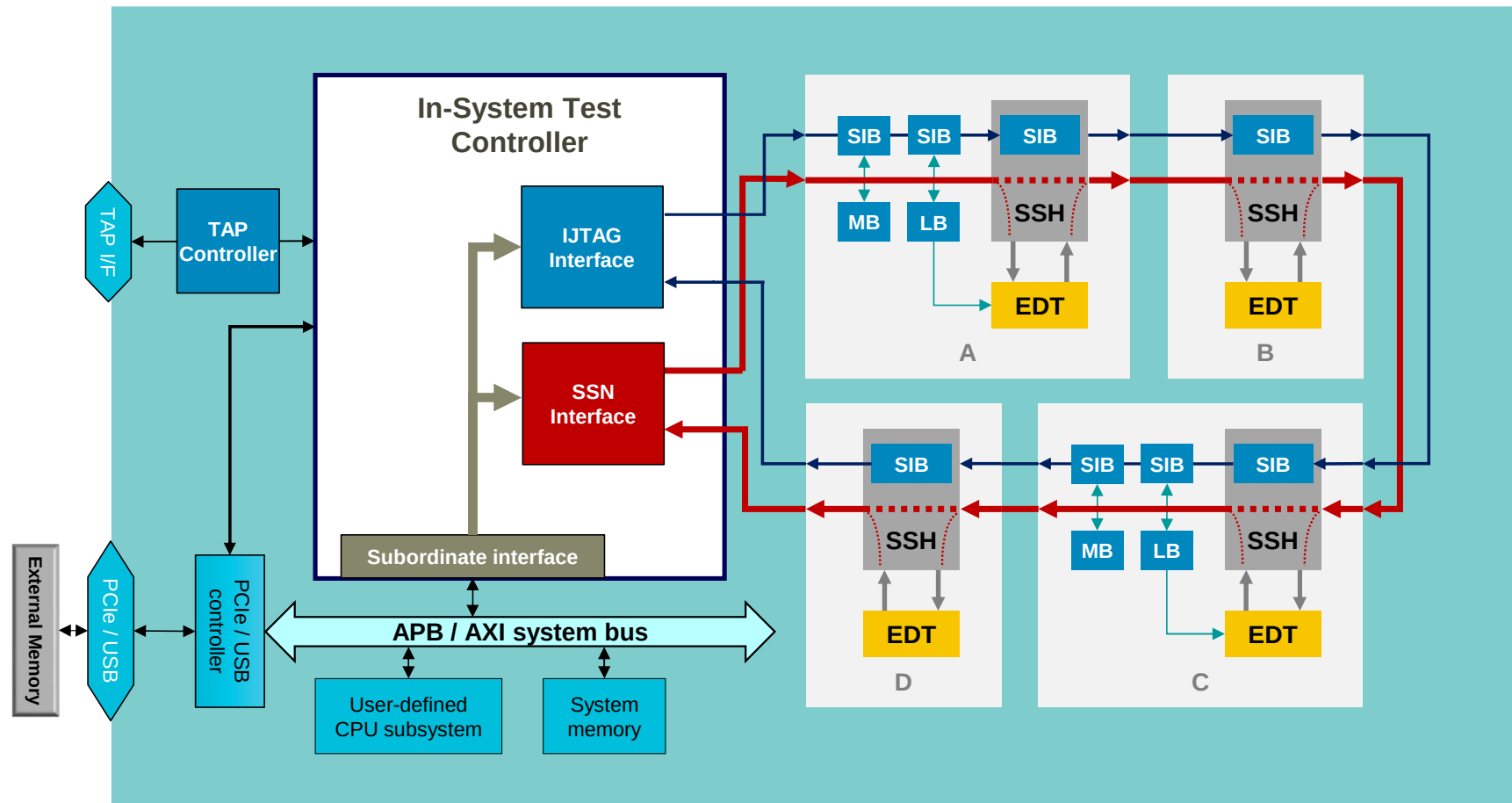
Tessent In-System Test more detailed view (6)



Tessent In-System Test more detailed view (7)

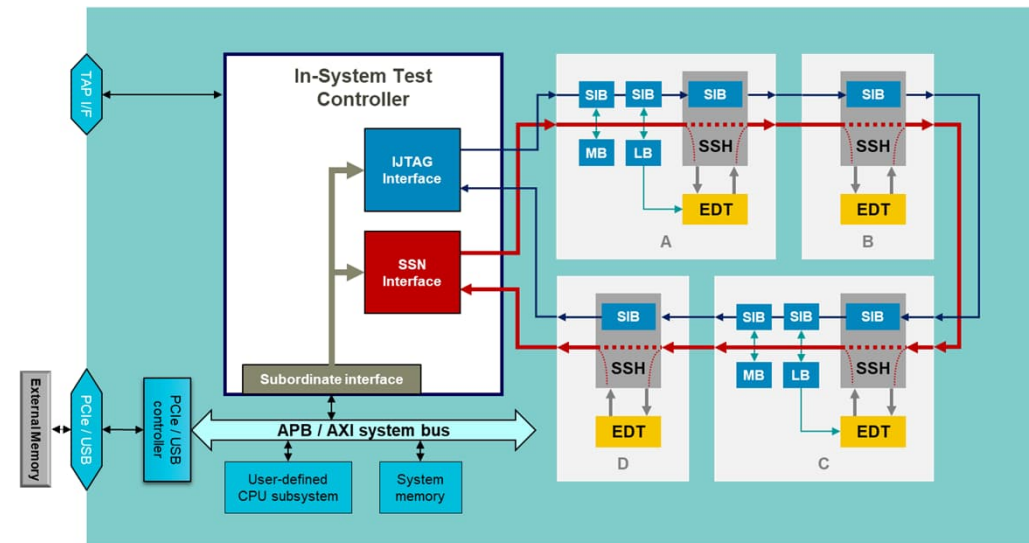


Tessent In-System Test more detailed view (8)



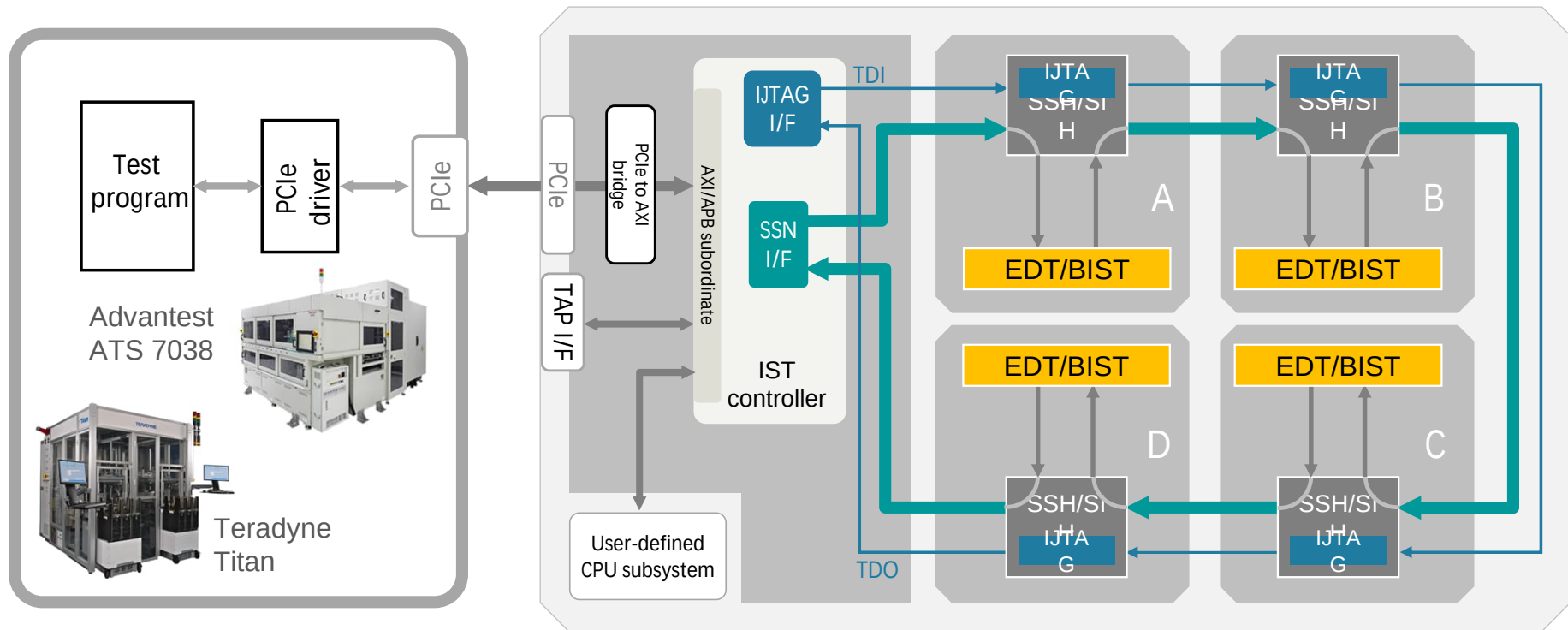
Tessent In-System Test *Superset of Tessent MissionMode*

- Support for IS-EDT patterns in addition to conventional Tessent MissionMode features
 - Such as LBIST, MBIST using IST-APB or MM DMA interfaces
- IS-EDT relies on a CPU to deliver test data
 - Deterministic patterns typically are stored off-chip to be accessed and controlled from the CPU
 - Advanced Peripheral Bus (APB) or Advanced eXtensible Interface (AXI) is connected to the CPU

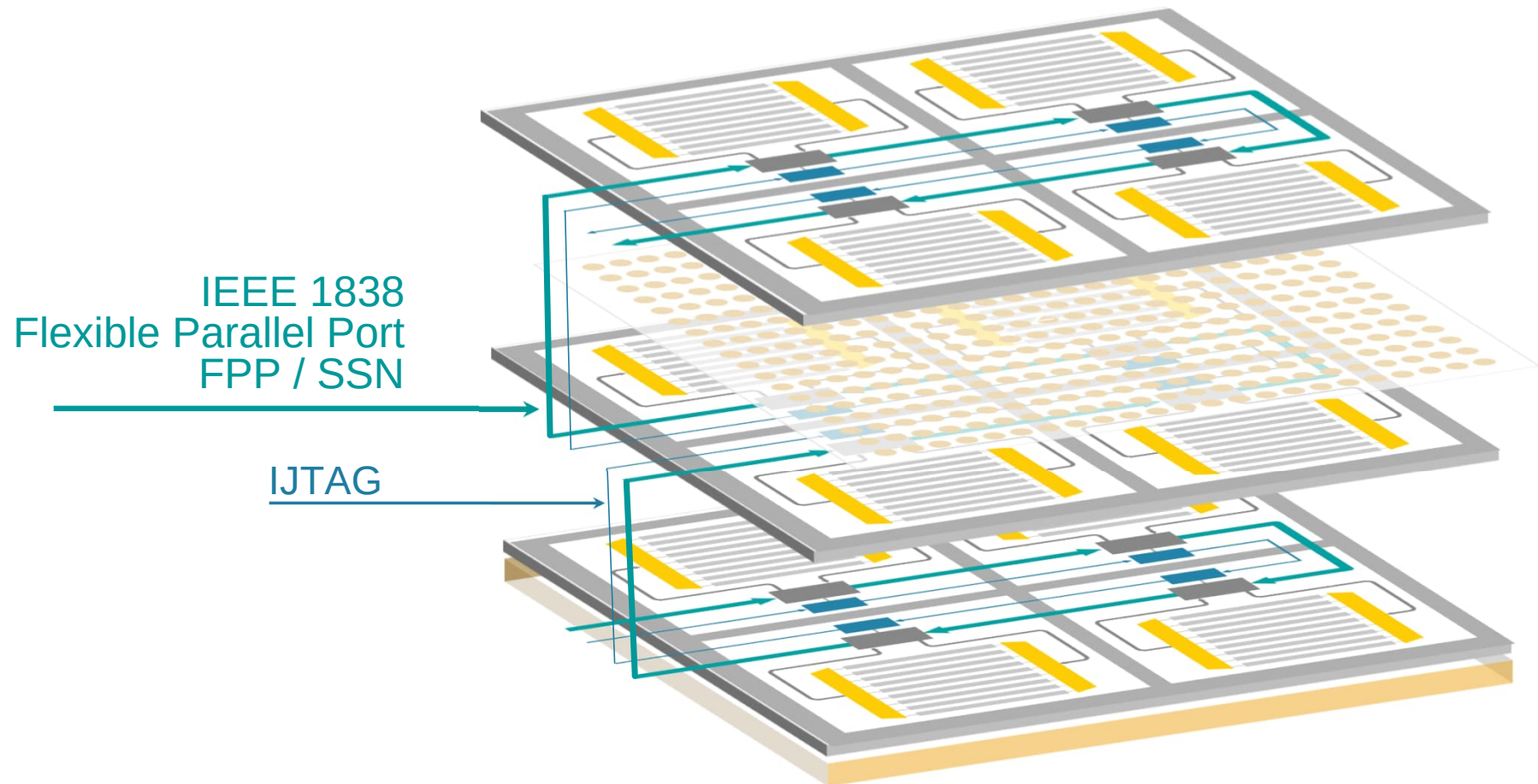


Structural system-level test (SLT)

Reusing the same infrastructure for SLT, significantly cheaper than ATE

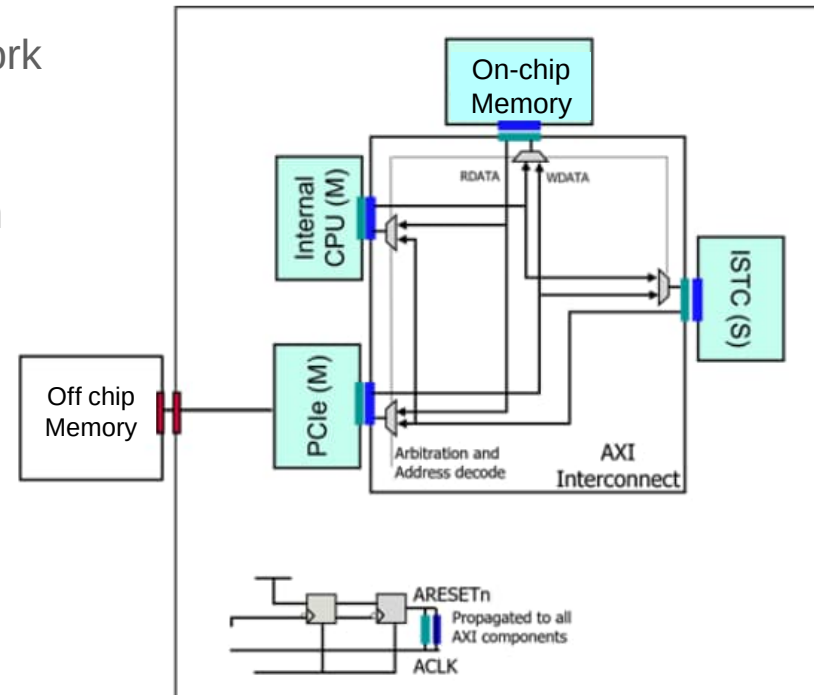


Implementing IEEE 1838 with SSN, IJTAG and In-System test



ISTC as AXI subordinate

- ISTC implemented as AXI subordinates can be used with the high-speed bus in DUT
- System components:
 - IST controller : drives the IJTAG and SSN network on the chip to perform manufacturing test or in-system test
 - Memory used by the CPU to store the in-system test data (and perform functional operations)
- Supports bus size up to 1024 bits
- Read/Write FIFOs to match bandwidth between AXI and SSN bus

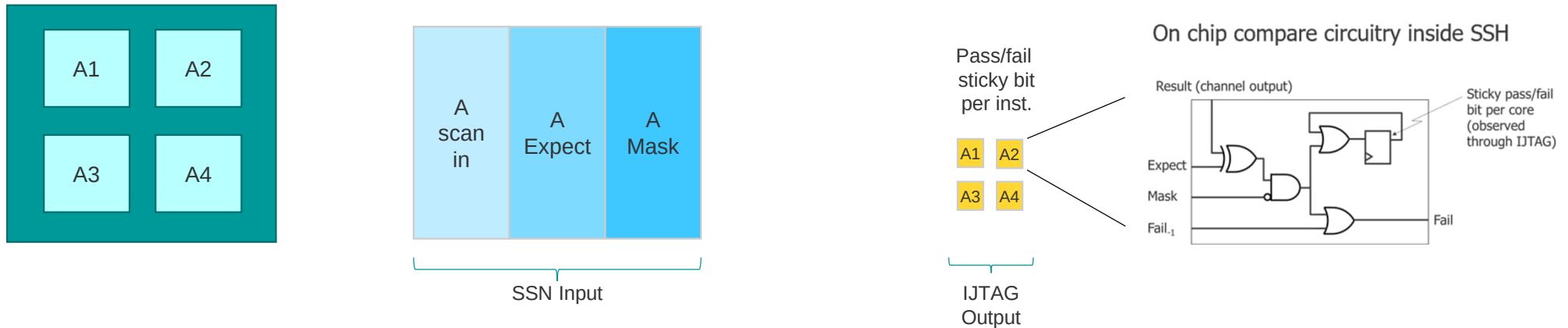


— AXI Manager Interface
— AXI Subordinate Interface
— PCIe Interface

(M) Manager Component
(S) Subordinate Component

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Diagnostics using on-chip compare (OCComp)



- Accumulated status can be disabled

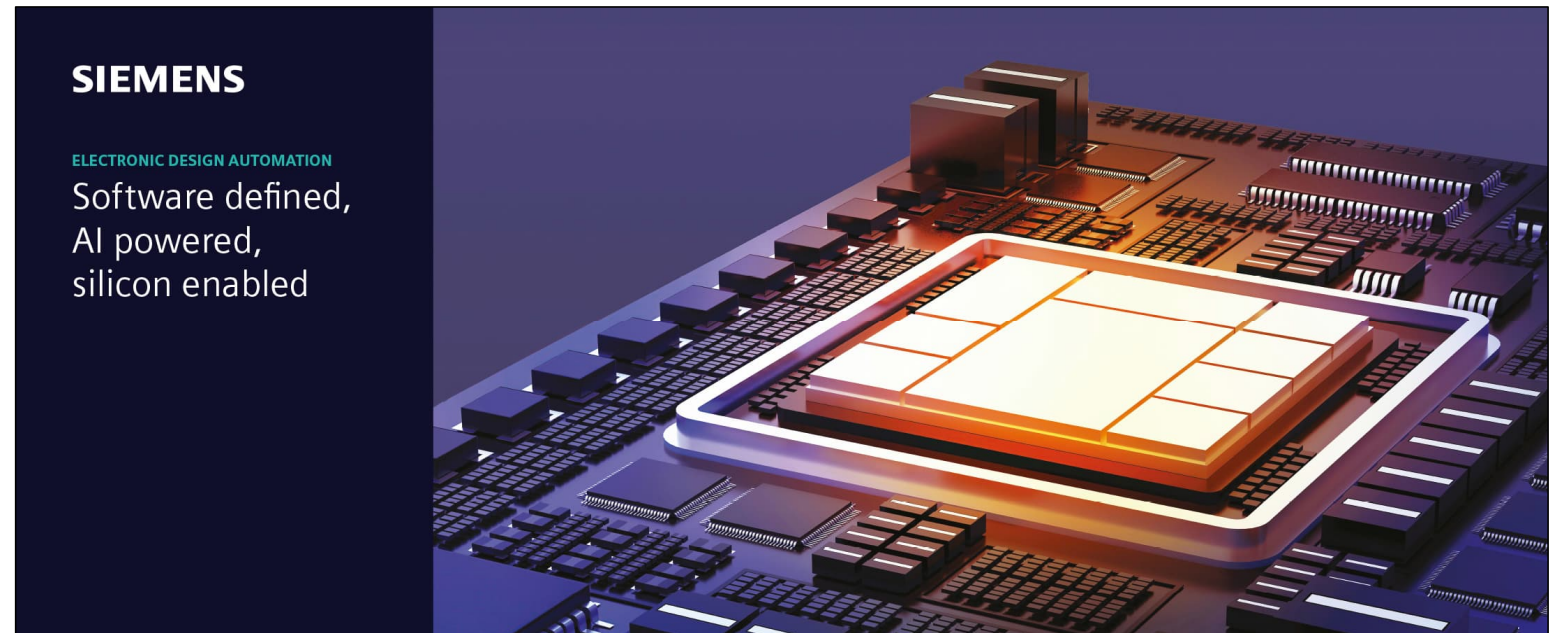
- Reduces test data volume/time for the set of identical cores by 1/4
- Only fail data is the pass/fail “sticky” bit per core scanned out through IJTAG at the end of pattern set
- Diagnosis requires a separate pattern set

Conclusions

- Market shifts towards SLM are causing greater adoption of in-system test methodologies
 - *Safety-minded customers are adopting advanced technology nodes*
 - *Quality-minded customers want to leverage existing on-chip infrastructure for in-system test*
- Many reasons exist for in-life device failures
 - *All reasons require in-system and in-field monitoring for errors*
- Tessent In-System Test, paired with Tessent Streaming Scan Network and Tessent TestKompress, are a valuable tool in detecting test escapes in-system and in-field
 - *Change test content to target new defects as failures are learned throughout the silicon lifecycle*
 - *Target specific defects related to silent data errors and aging with deterministic tests*

Come visit

- Come and visit us in the Expo!
- You can find us at booth 7+8:



Thank you!

For more information about this presentation, please contact
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