Smart NoC Automation: Accelerating AI-Ready SoC Design in the Era of Chiplets

Semilsrael 2025

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11 November, 2025

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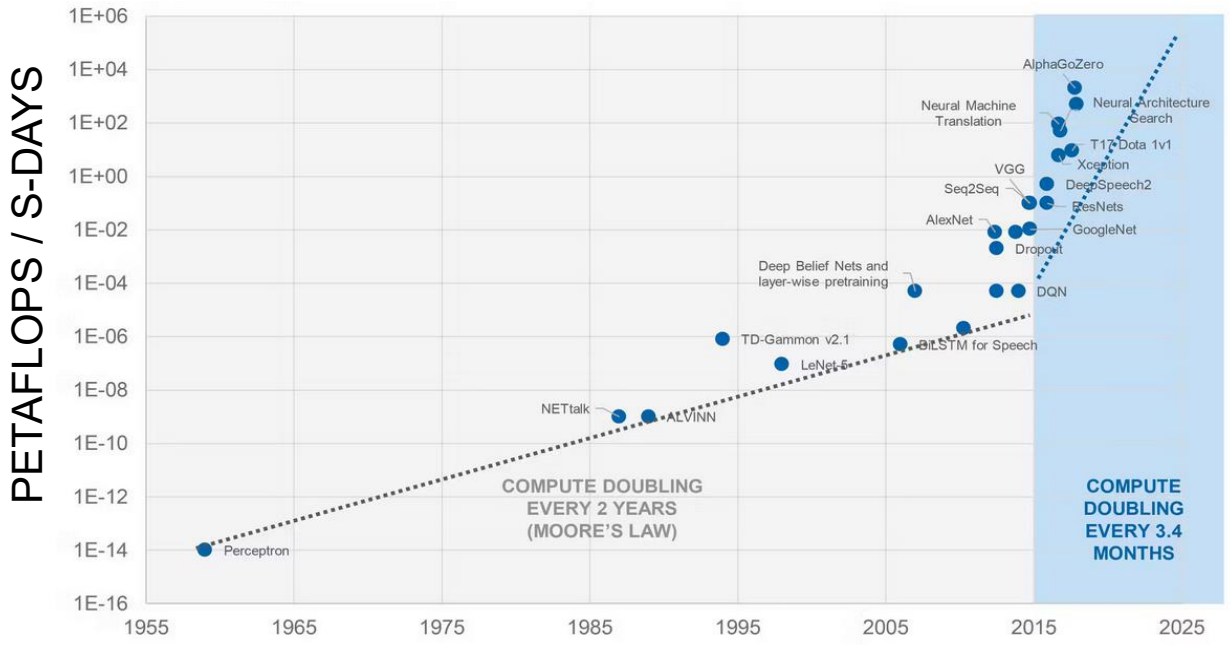
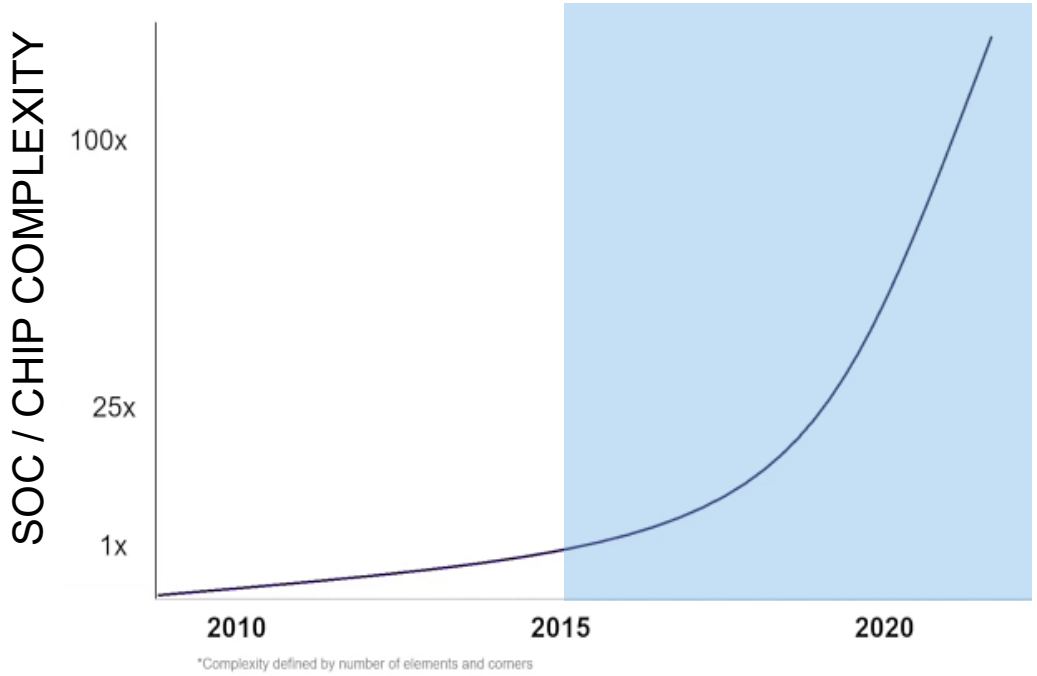
Era of AI Compute: 7x Acceleration → Rising SoC Complexity

More logic and design constraints further complicating on-chip connectivity (“the glue”)

AI Era of Compute: 7x Acceleration



Driving Exponential Chip Complexity



Modern silicon chips are connected by **billions of wires**, ever-expanding with growing complexity
→ **more & bigger networks-on-chip, with more complex architecture / topology setup**

Sources: OpenAI: AI and Compute Research Report, Semi Engineering, Synopsys

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The Hidden Challenge: Efficient Data Movement

Edge AI Application

"The MAX78000's performance is heavily memory-bound,
with memory I/O consuming up to 90% of total inference time."
(hackster.io)

Product Ideas

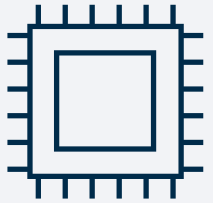
Network-on-Chip Connectivity

Responsible for overall chip performance and power efficiency

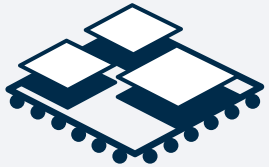
Architecture Exploration

Design & Verification

Implementation & Validation



End Designs



Data Center AI Application

"Data movement dominates the dynamic energy consumption of
the GPU (up to 84%), with DRAM accesses being the main contributor."
(computer.org)

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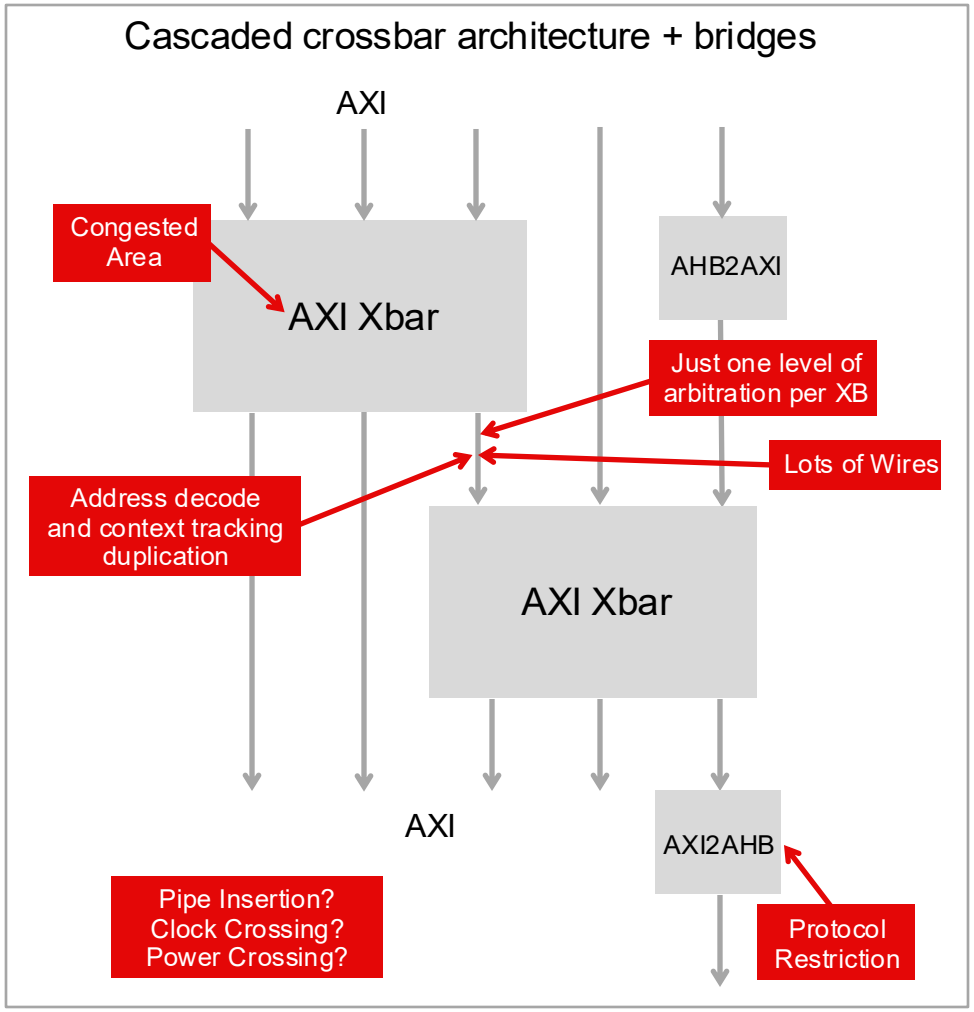
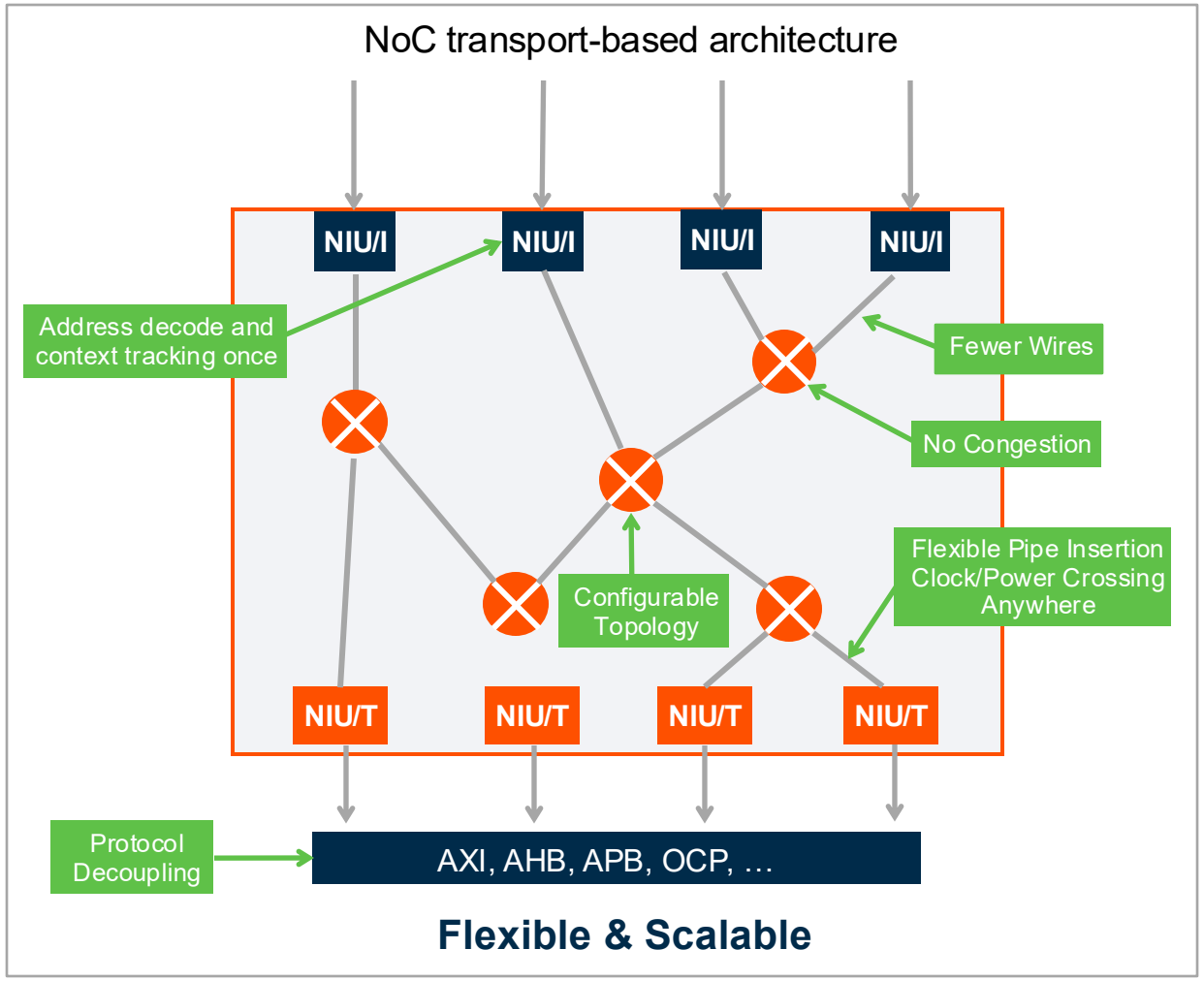
NoC technology is better than cascaded crossbars





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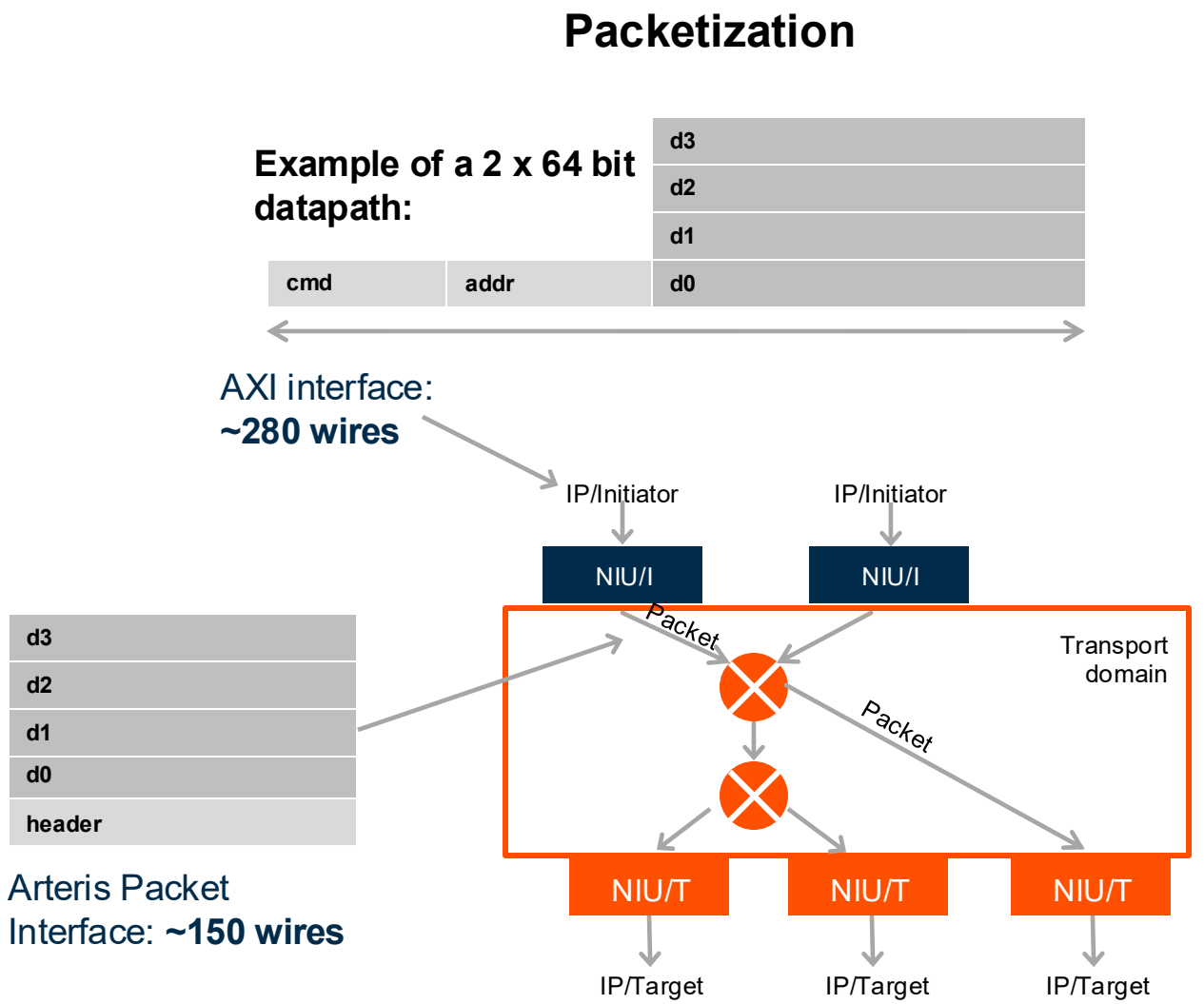
NoCs Packetize data to reduce wires, lowering power consumption

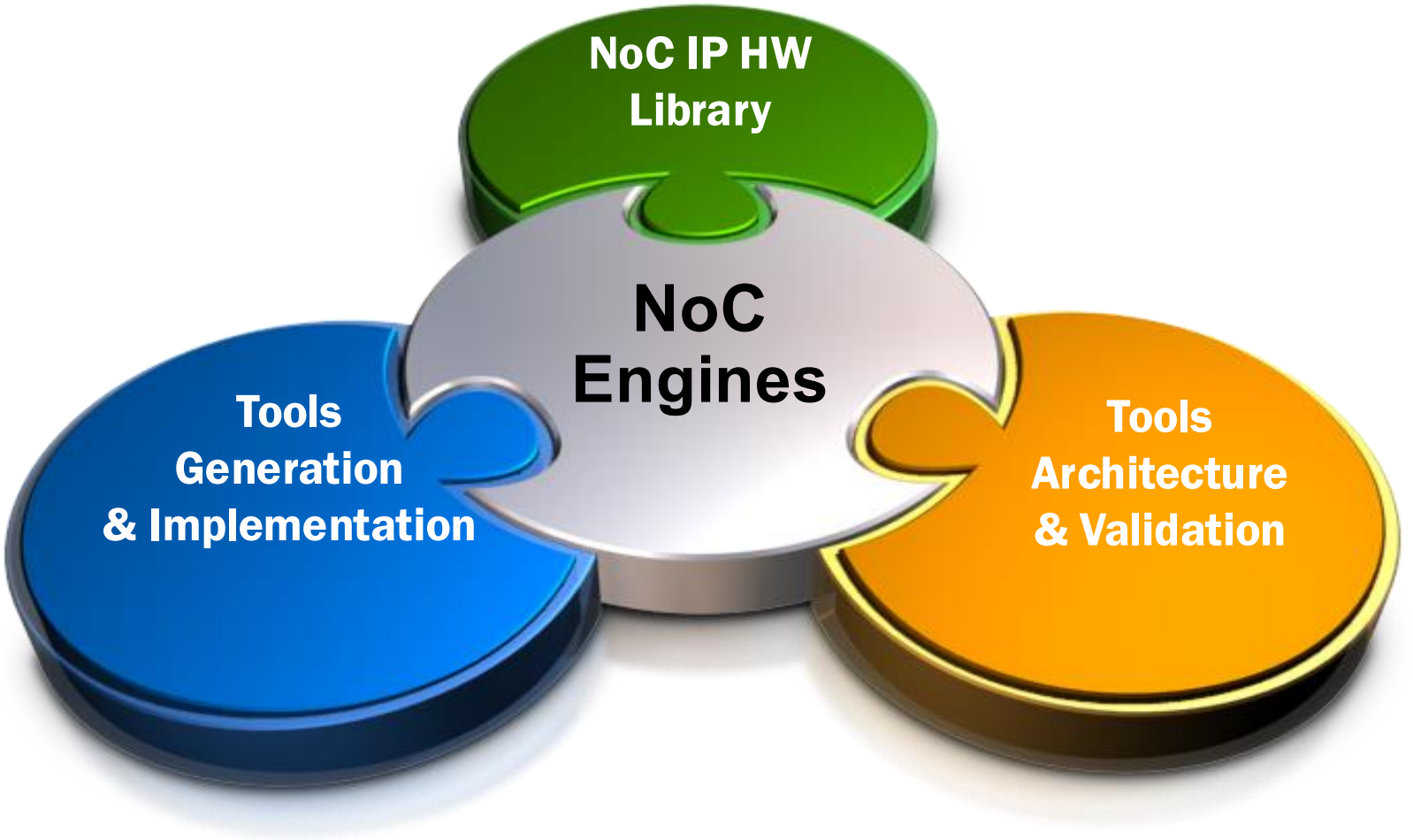
- Reduce routing congestion
  - Packetization – fewer wires
- Ease timing closure
  - Fine grain pipeline stage insertion
- Reduce die area
  - Simpler datapath logic
- Reduce active power
  - Unit-level dynamic clock gating
- Decouple sockets from transport
  - Easier integration



Spoiler

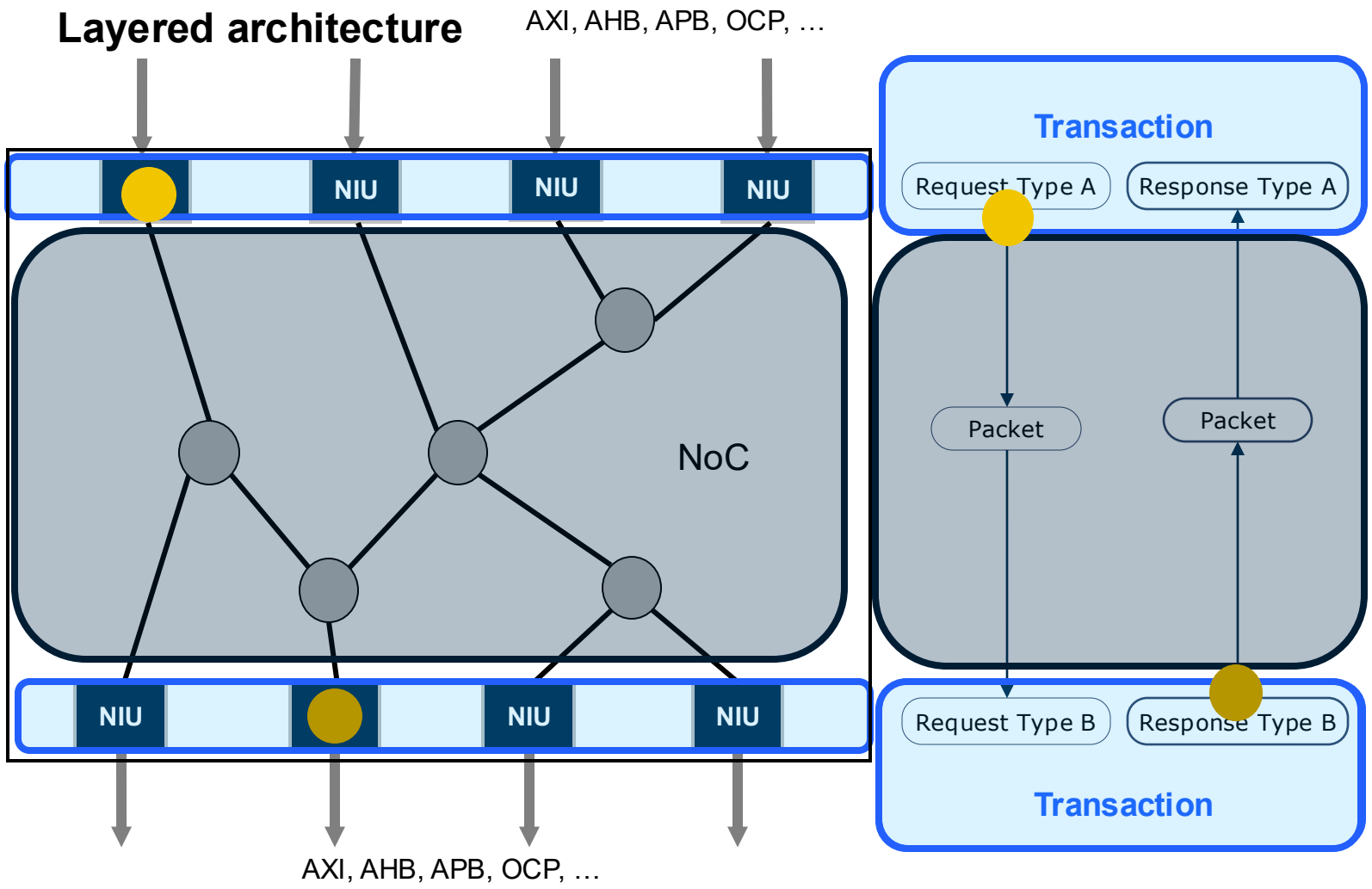
Not all NoCs are Equal!

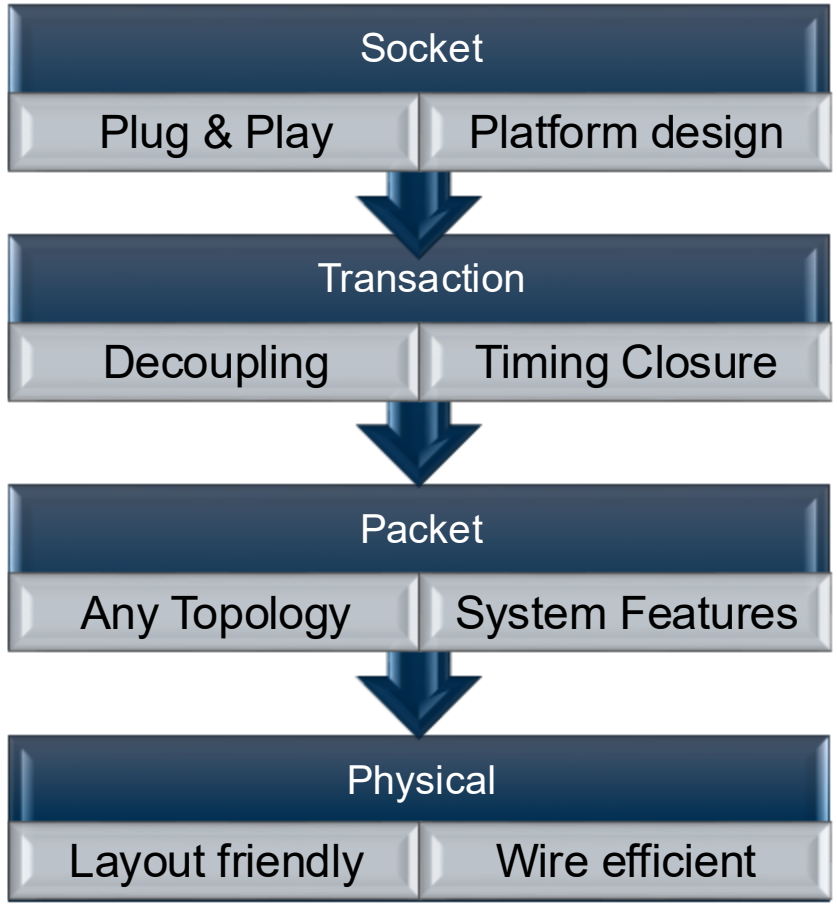
Smart NoC Solution



Requires a Layered Approach to Network on Chip Design

Layered architecture





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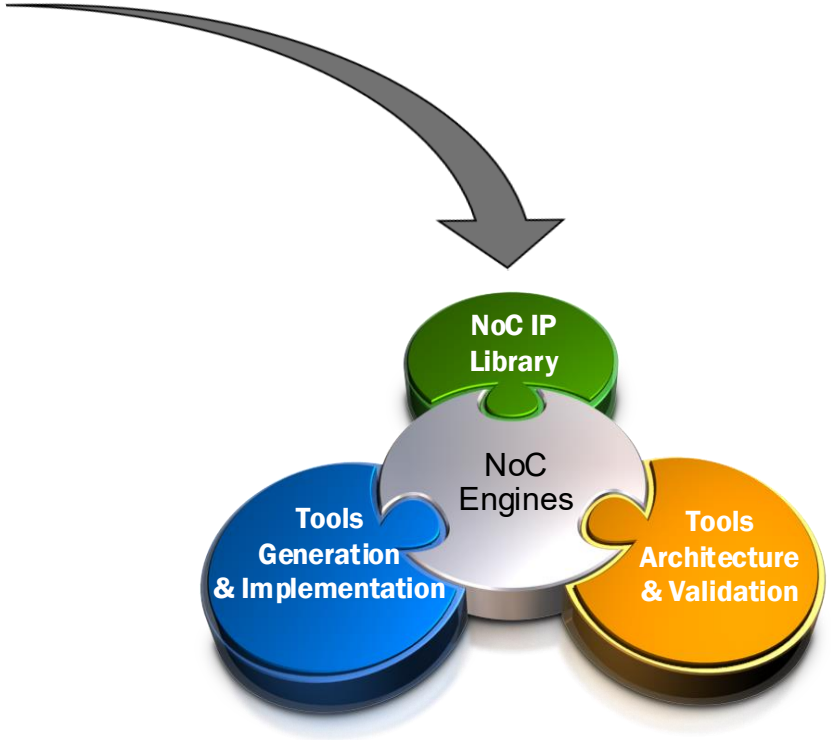
Requires a Mature IP Library of Small Units

For flexible and scalable designs

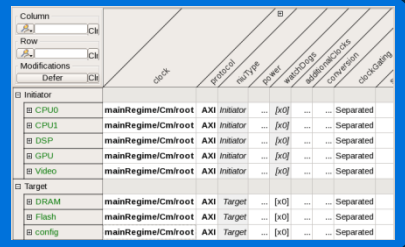
Category	Library units
NIU (Network Interface Units)	**ACE-Lite, AXI, AHB, APB, PIF, OCP, others**
Transport	mux, demux, serializer, buffer
Domain adapter	sync/async clock, power, voltage
Timing	pipeline stage
QoS	dynamic priorities, bandwidth limiter/regulator
Re-order Buffer	manager for out-of-order memory responses
Security	user defined firewalls
Debug	error, statistics, trace probes
Interchip link	FPGA link, PSI, LLI
Resilience/Safety	timeout, safety controller, checkers



Requies a Methodology – Specify, Architect, Generate and Verify

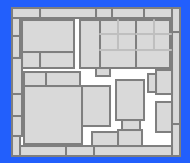
Floorplan Outline

Specification
sockets
domains
memory map

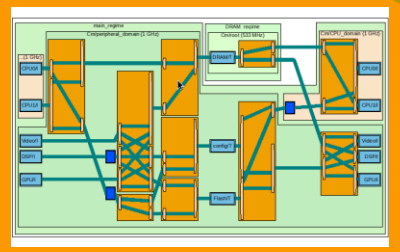


Traffic Scenario

Physical Awareness
LEF/DEF,
auto pipe,
placement

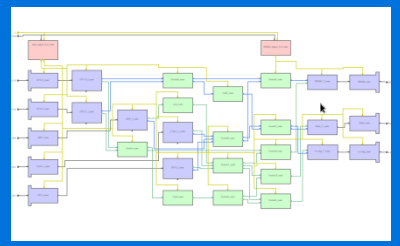


Architecture
switch topology
QoS, buffers
serialization



FlexExplorer (SystemC)
use case performance

Structure
RTL, SystemC
IP-XACT
scripts/constraints



EDA P&R Flow

EDA Synthesis Flow

Gate Estimates

Verification Testbench

Smart NoC Technologies

Designer input

Constraints
Interfaces
Memory Map
Safety
Floorplan

Intent
Perf & QoS
Domain
Debug
Security

NoC Tools

Capture
Constraints & Intent

User Interface
Back annotation

Collateral export

NoC Engines

Generation
Topology creation

Timing solving
Pipeline insertion

Assembly
Parameters resolution

Estimation
Timing & Area

Creation
Verilog & SV & Doc

NoC Libraries

NoC System IP Library
NoC IP Library
Protocols

Foundation library

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Smart NoC Design Flow

Specification + performance intent + physical constraints = topology generation

Step 1

- Create a Network-on-Chip **specification**
- Assign initial high-level performance parameters
- **Verify performance** with architectural model and simulation

Step 2

- Capture virtual **floor planning** constraints and specify **performance intent**
- **Smart NoC** generates Network-on-Chip topology
- **Verify performance** with architectural model and simulation

Step 3

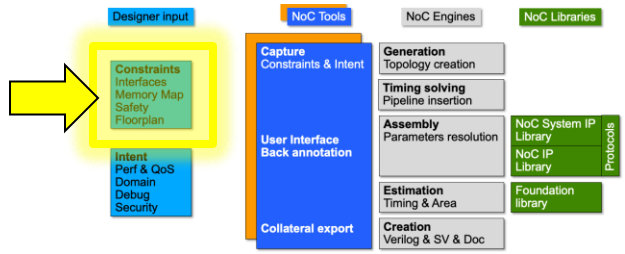
- Insert **pipeline** slice with built in Static Timing Analysis (STA) engine
- **Verify performance** with architectural model and simulation

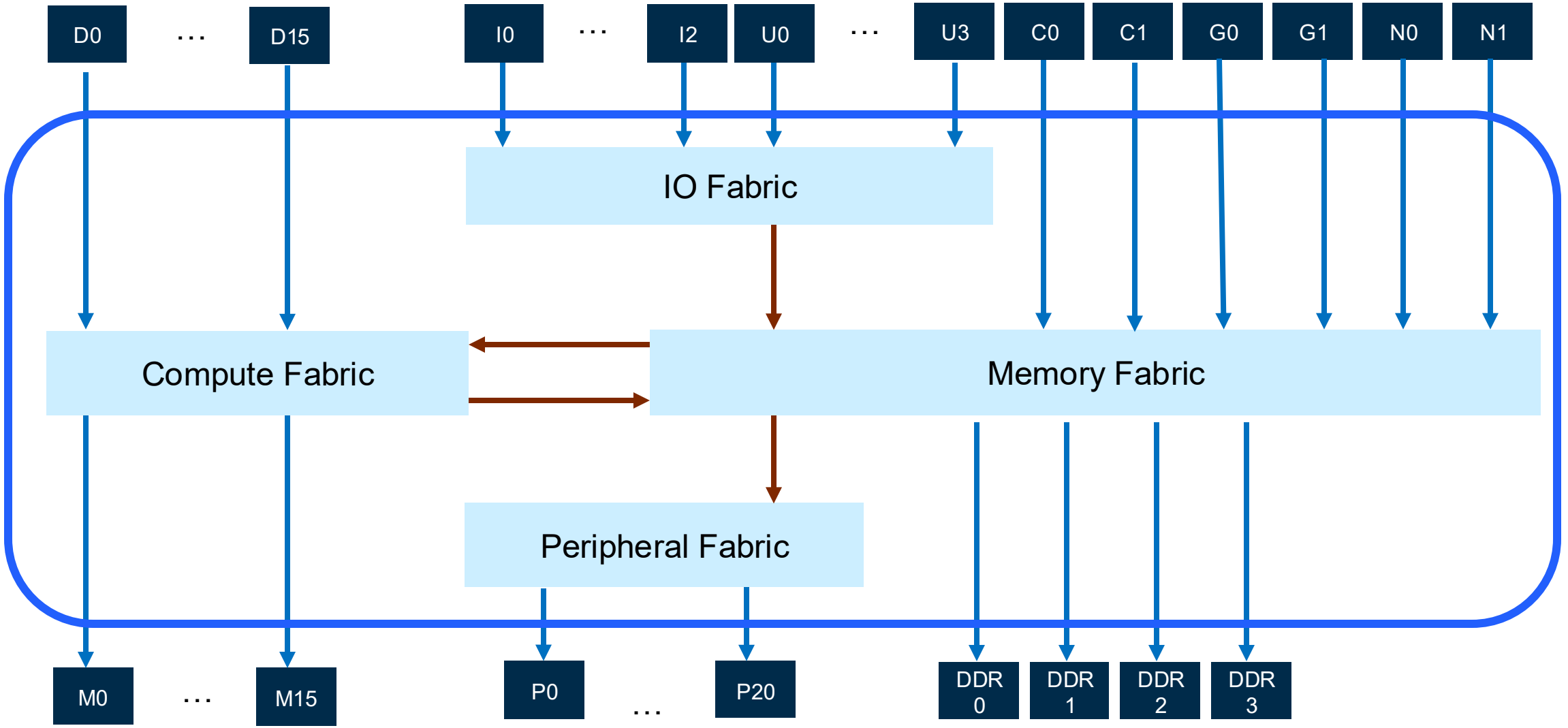
Step 4

- Create a physical synthesis **framework**
- Validate with physical synthesis tools using Smart NoC **constraints**

Step 1 Network-on-Chip Integration Specification

Block diagram: 79 interfaces ; 7 clocks ; 1 GHz ; 32 to 128 bits





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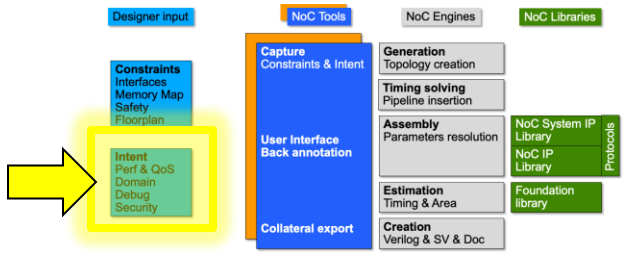
Step 1 Network-on-Chip Performance Requirements & Physical Constraints

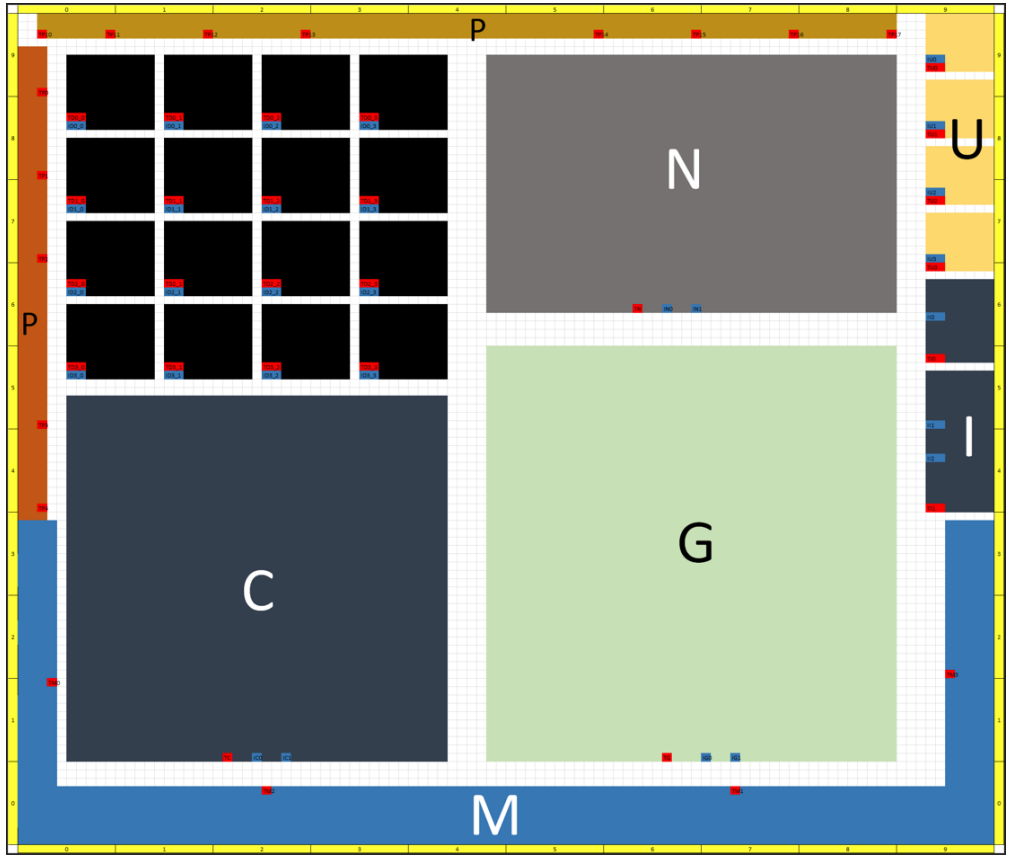
60 GB/s aggregate traffic; 10 mm x 10 mm die ; 14 nm ; 1 GHz



Bandwidth and QoS Requirements

- Compute accelerators:
  - 7 GB/s each across all TCM
  - 250 MB/s each toward DDRs
- C: 12 GB/s -> DDRs
- G: 12 GB/s -> DDRs
- N: 12 GB/s -> DDRs
- U: 8 GB/s -> DDRs
- I: 1.5 GB/s -> DDRs

Blockages & Socket Positions



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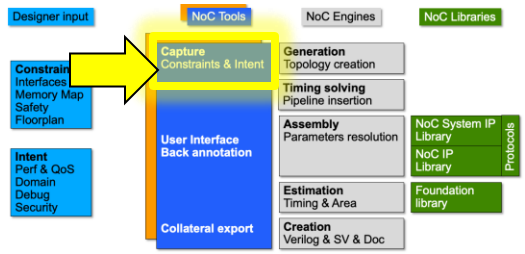
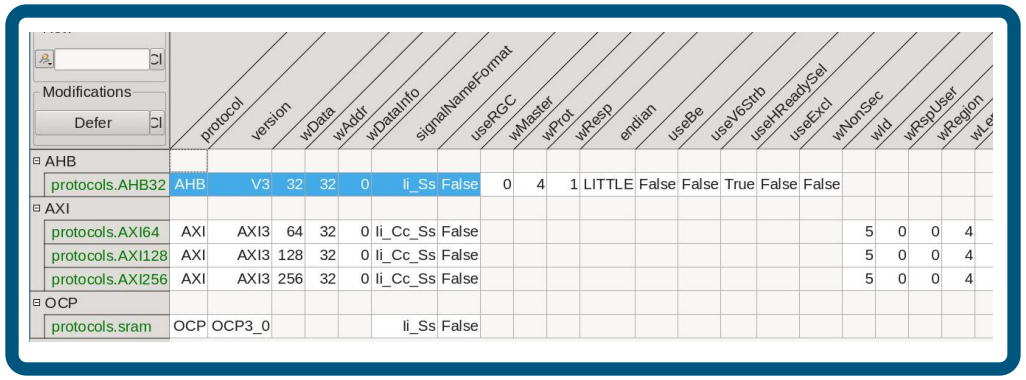
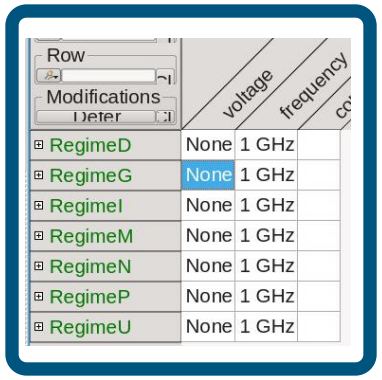
Step 1 Enter Specification in NoC Tools

Easy table base capture of the specification

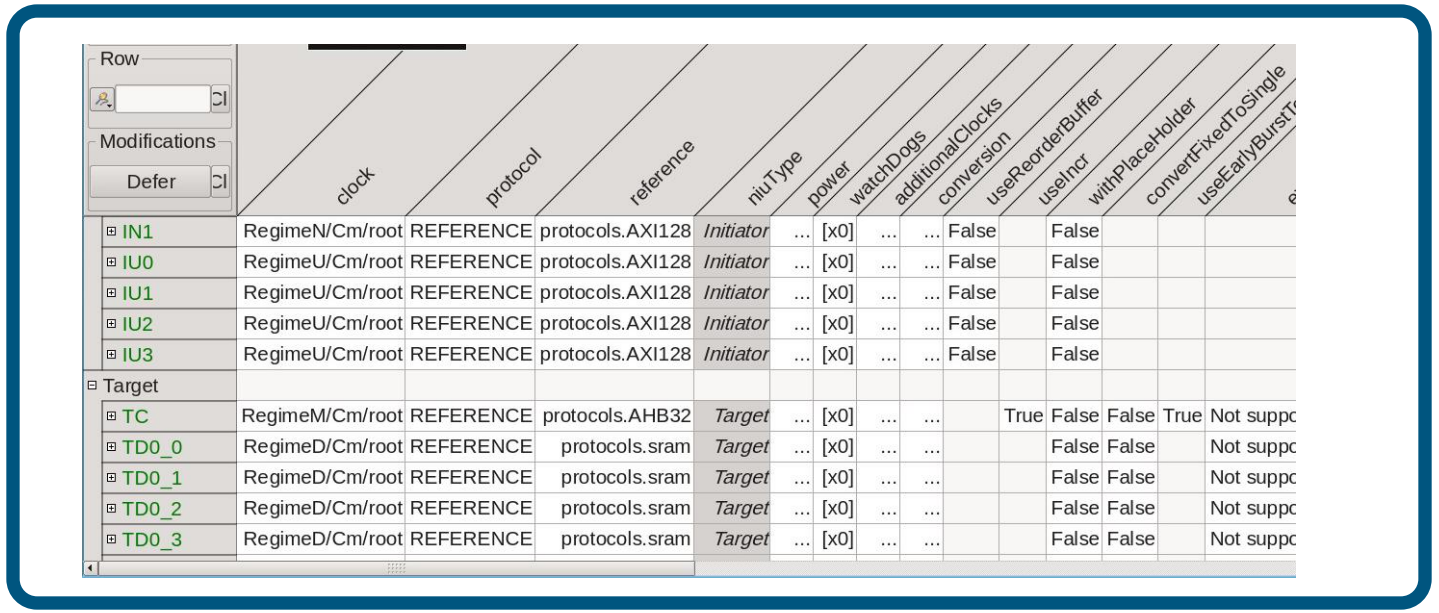




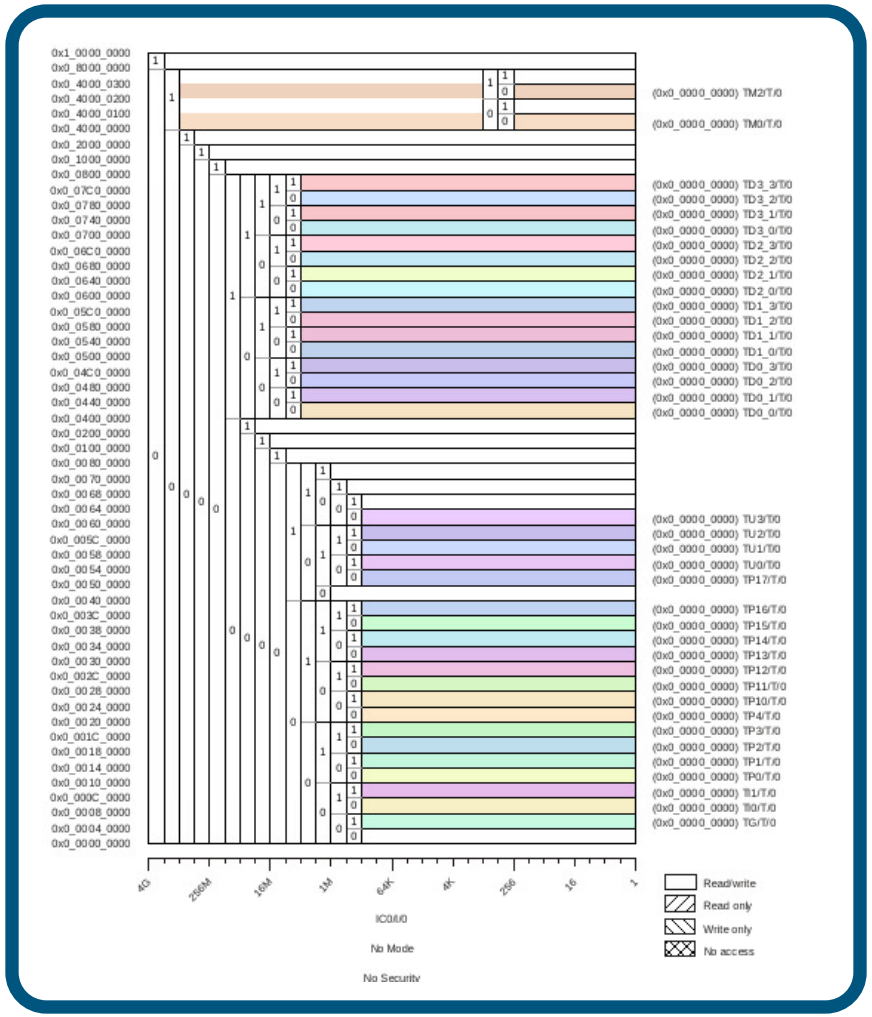
	protocol	version	wData	wAddr	wDataInfo	signalNameFormat	useRGC	wMaster	wProt	wResp	endian	useBe	useV6Strb	useHReadySel	useExcl	wNonSec	wId	wRspUser	wRegion
AHB																			
protocols.AHB32	AHB	V3	32	32	0	Ii_Ss	False	0	4	1	LITTLE	False	False	True	False	False			
AXI																			
protocols.AXI64	AXI	AXI3	64	32	0	Ii_Cc_Ss	False									5	0	0	4
protocols.AXI128	AXI	AXI3	128	32	0	Ii_Cc_Ss	False									5	0	0	4
protocols.AXI256	AXI	AXI3	256	32	0	Ii_Cc_Ss	False									5	0	0	4
OCP																			
protocols.sram	OCP	OCP3_0				Ii_Ss	False												



	voltage	frequency
RegimeD	None	1 GHz
RegimeG	None	1 GHz
RegimeI	None	1 GHz
RegimeM	None	1 GHz
RegimeN	None	1 GHz
RegimeP	None	1 GHz
RegimeU	None	1 GHz

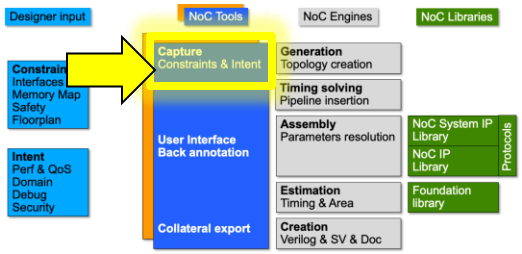


	clock	protocol	reference	niuType	power	watchDogs	additionalClocks	conversion	useReorderBuffer	useIncr	withPlaceHolder	convertFixedToSingle	useEarlyBurstT
IN1	RegimeN/Cm/root	REFERENCE	protocols.AXI128	*Initiator*	...	[x0]	...	...	False		False		
IU0	RegimeU/Cm/root	REFERENCE	protocols.AXI128	*Initiator*	...	[x0]	...	...	False		False		
IU1	RegimeU/Cm/root	REFERENCE	protocols.AXI128	*Initiator*	...	[x0]	...	...	False		False		
IU2	RegimeU/Cm/root	REFERENCE	protocols.AXI128	*Initiator*	...	[x0]	...	...	False		False		
IU3	RegimeU/Cm/root	REFERENCE	protocols.AXI128	*Initiator*	...	[x0]	...	...	False		False		
Target													
TC	RegimeM/Cm/root	REFERENCE	protocols.AHB32	*Target*	...	[x0]	...	...		True	False	False	True
TD0_0	RegimeD/Cm/root	REFERENCE	protocols.sram	*Target*	...	[x0]	...	...			False	False	
TD0_1	RegimeD/Cm/root	REFERENCE	protocols.sram	*Target*	...	[x0]	...	...			False	False	
TD0_2	RegimeD/Cm/root	REFERENCE	protocols.sram	*Target*	...	[x0]	...	...			False	False	
TD0_3	RegimeD/Cm/root	REFERENCE	protocols.sram	*Target*	...	[x0]	...	...			False	False	

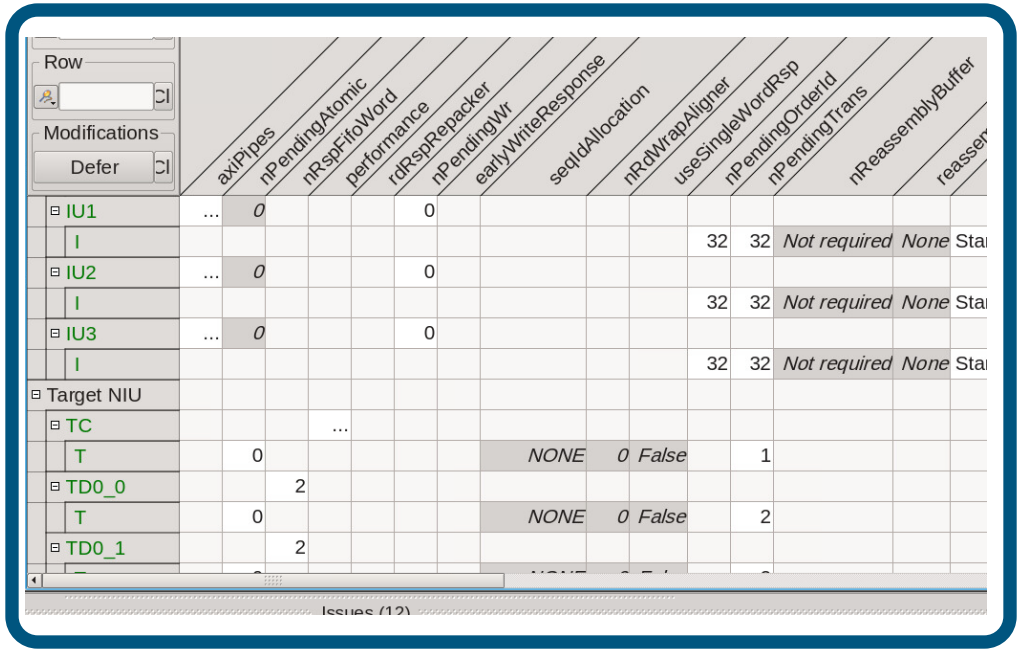


Step 1 Assign Initial High-Level Performance Parameters

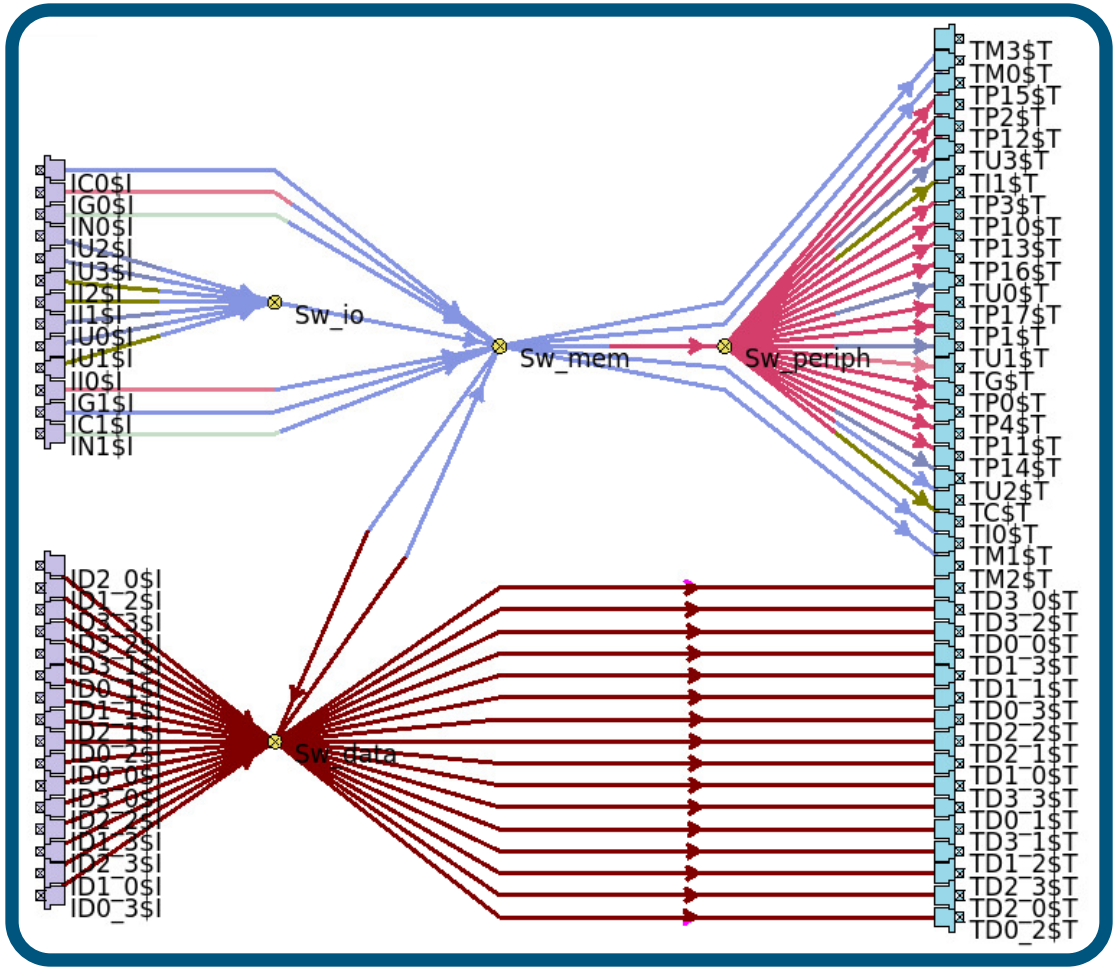
Keep it simple, a complex topology must be floorplan-driven



NIU performance parameters



Start with a simple crossbar-based topology



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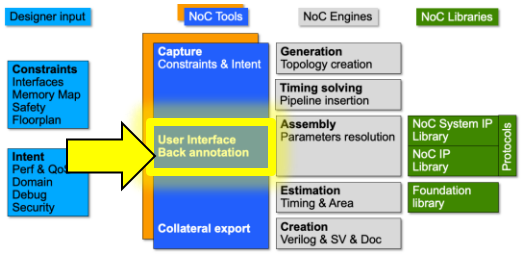
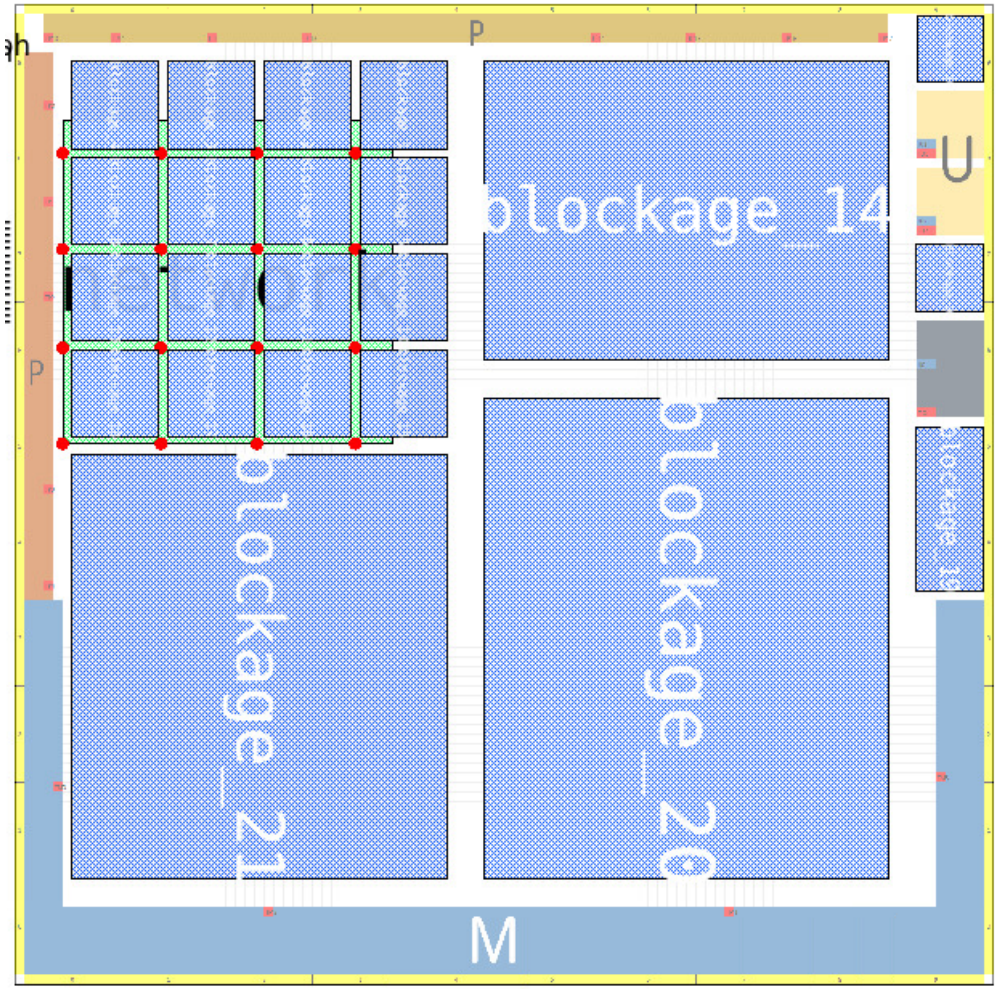
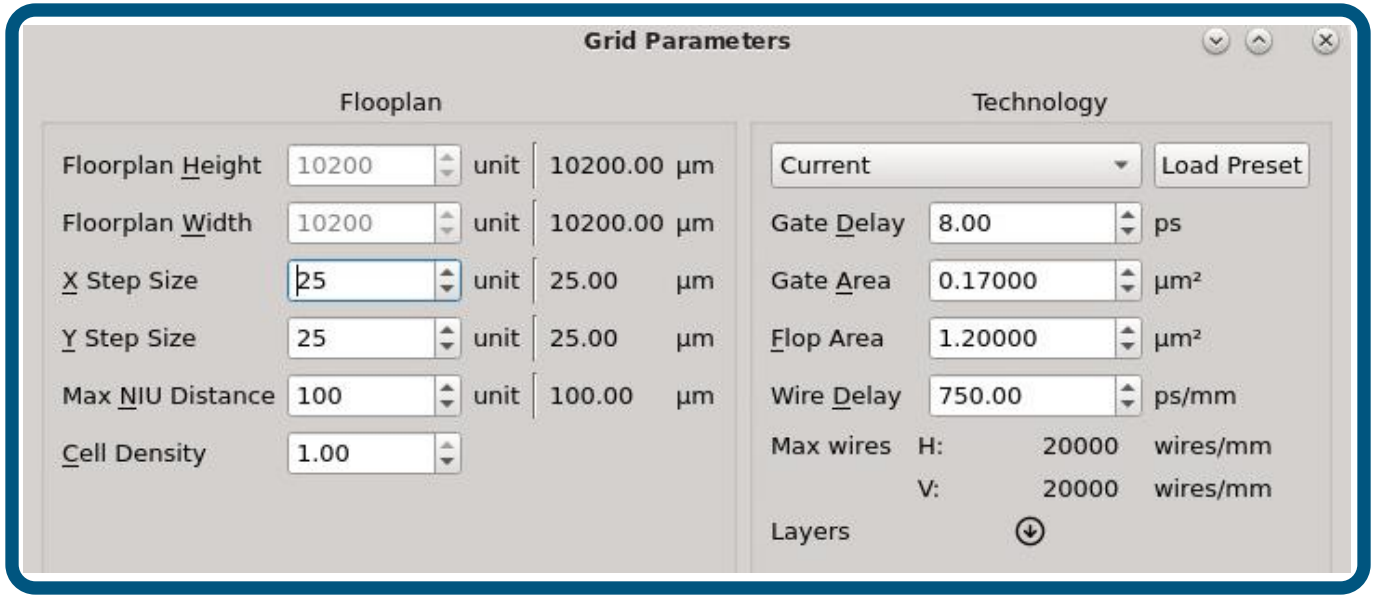
Step 2 Capture Physical Constraints

Blockages and technology library modeling

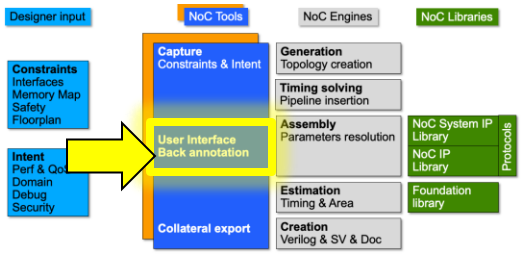


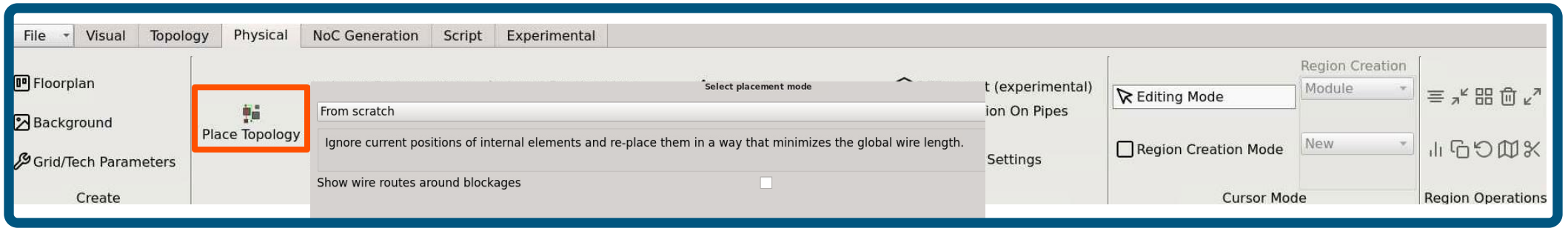


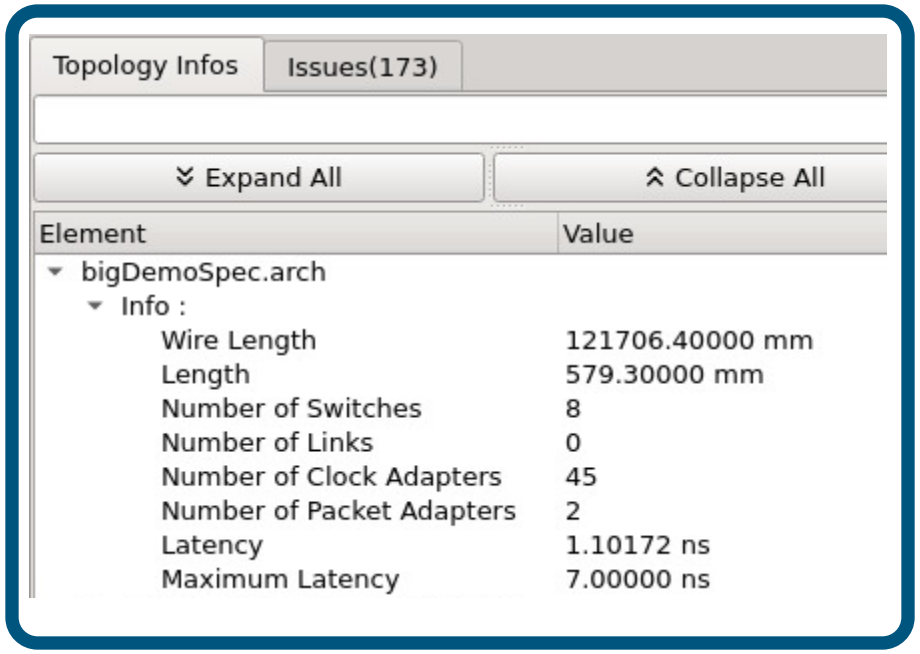


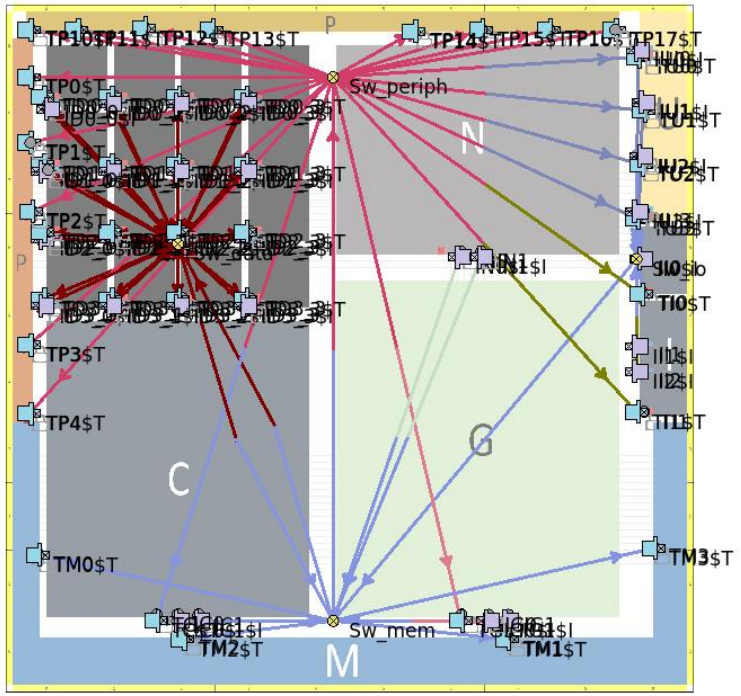
Step 2 NoC Generation

Initial topology versus floorplan









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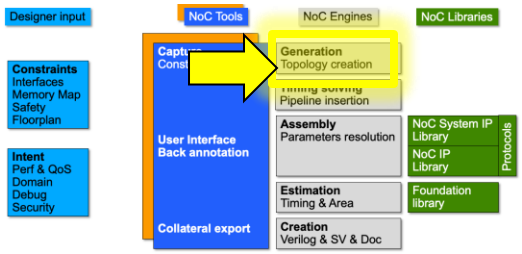
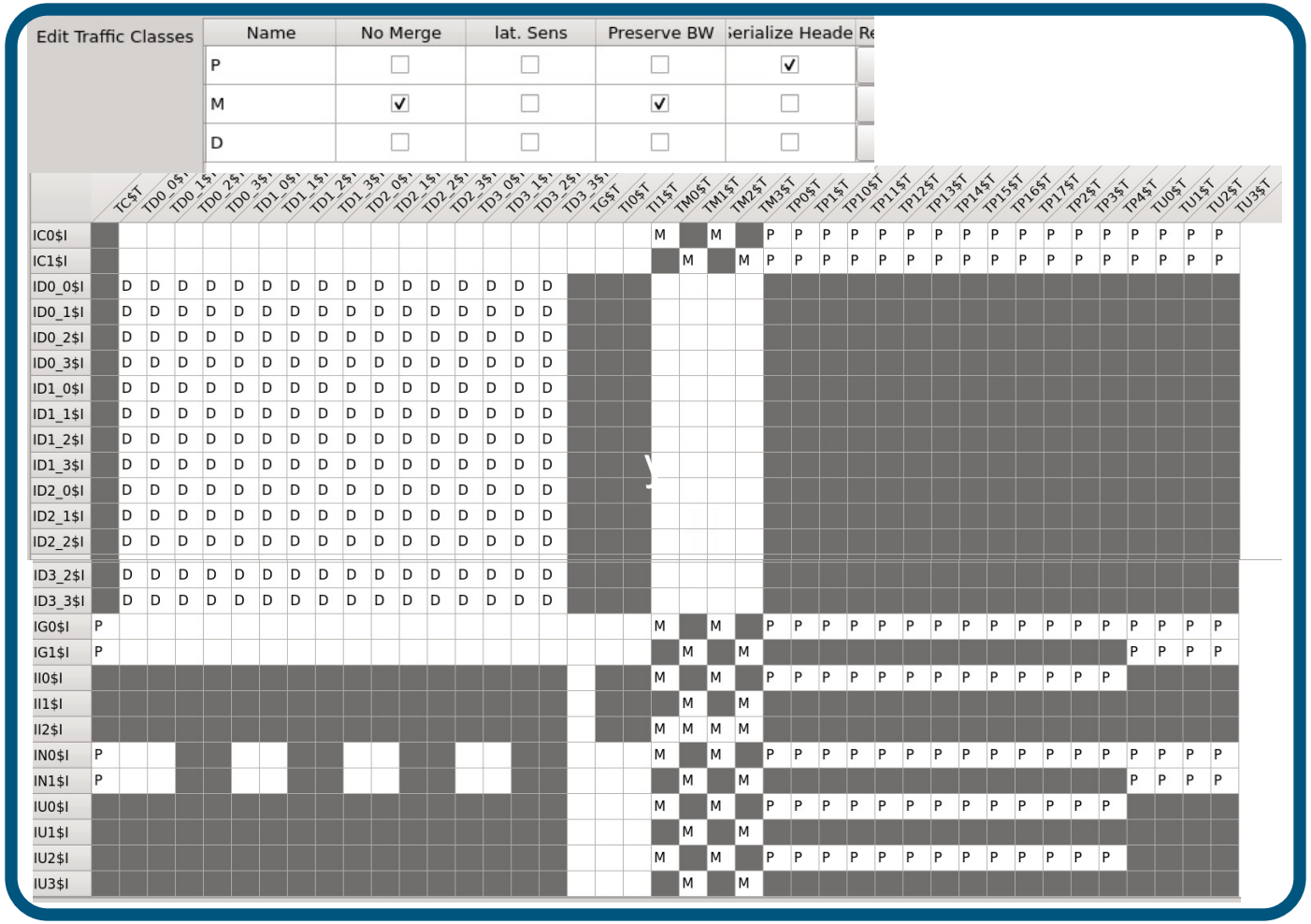
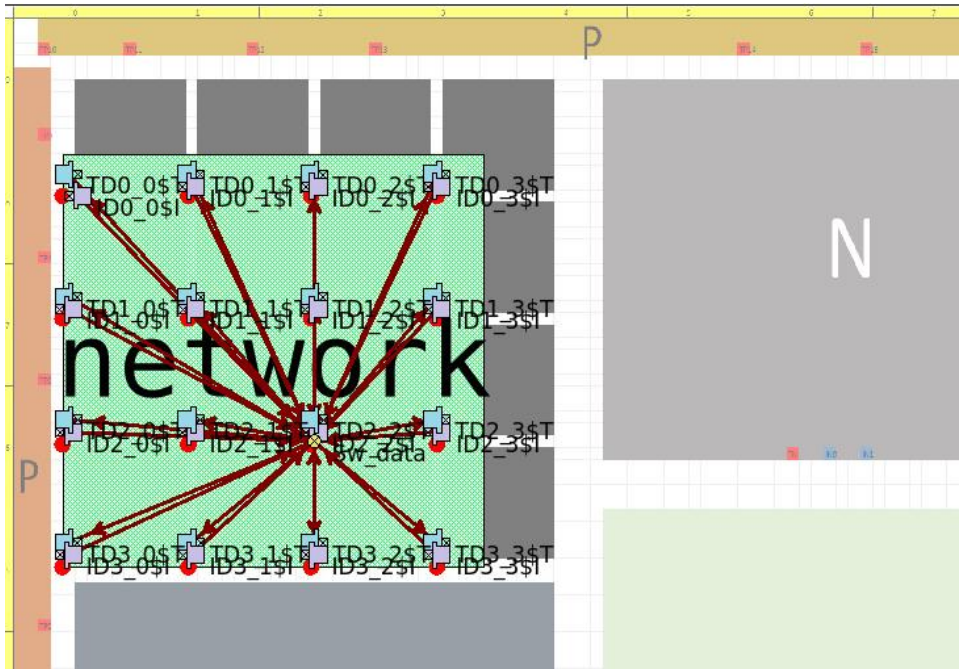
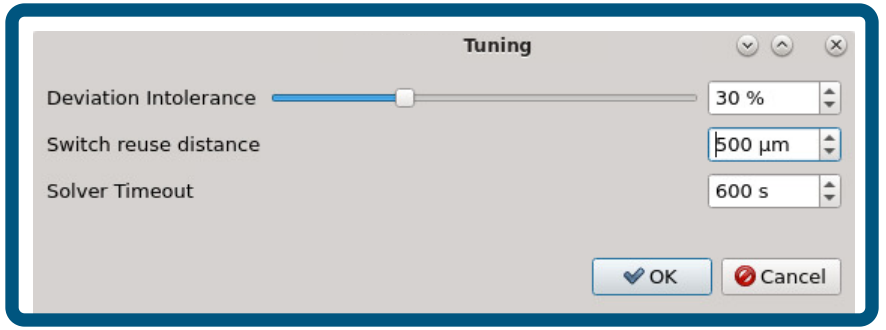
Step 2 NoC Generation

Specify performance intent



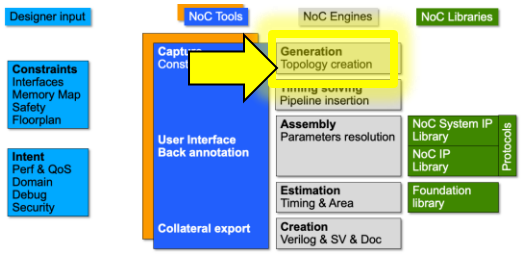




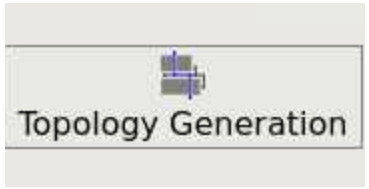


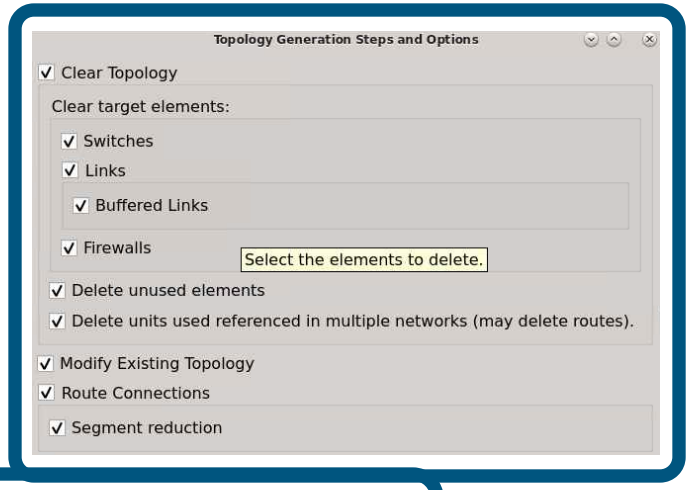
Step 2 NoC Generation

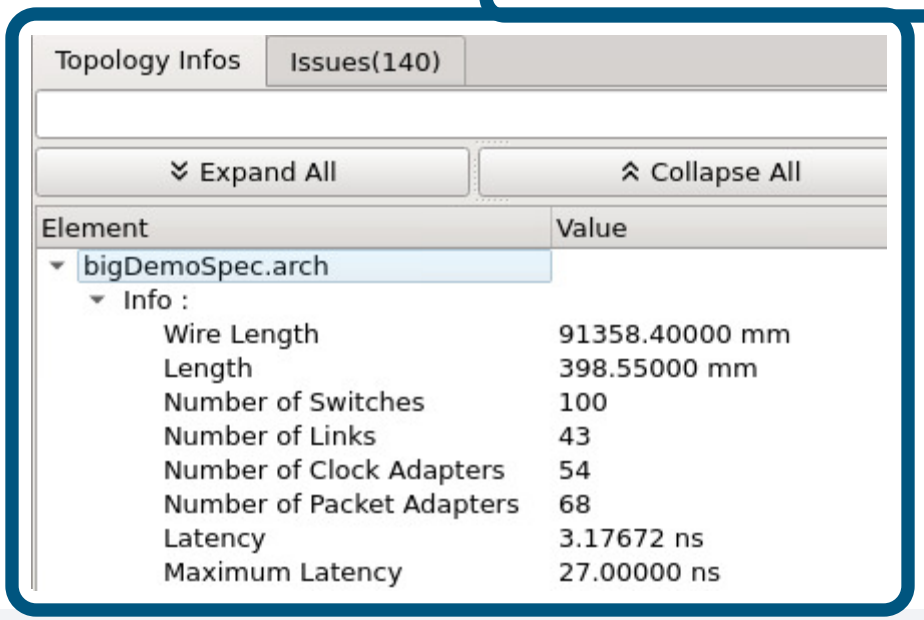
Generates optimized NoC topology, automatically minimizing wire length

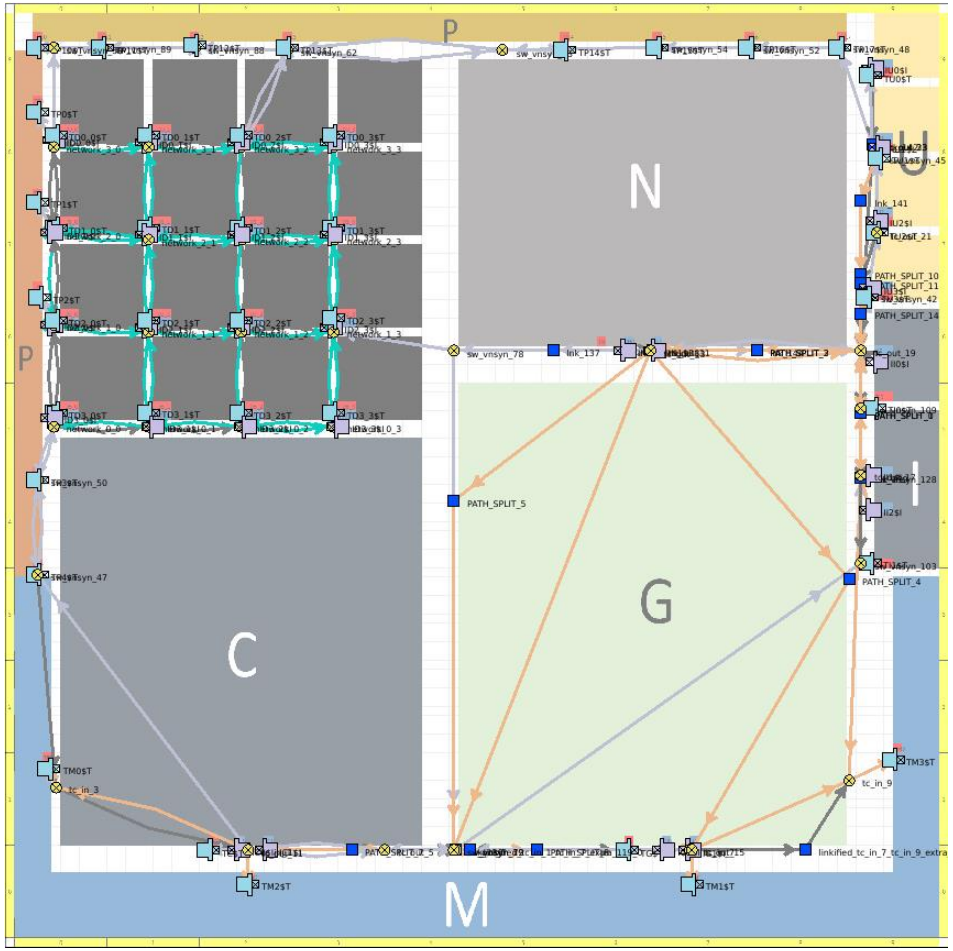


2 minutes…









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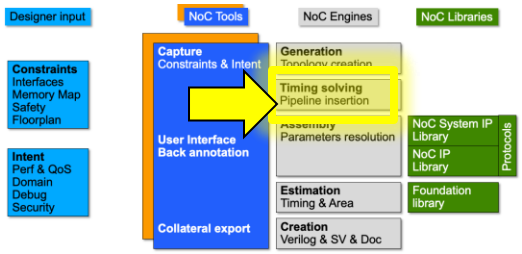
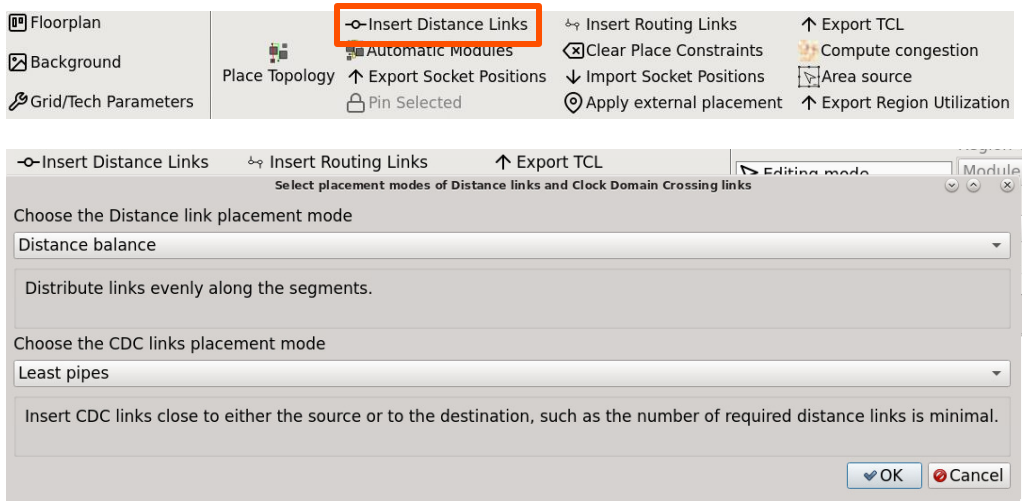
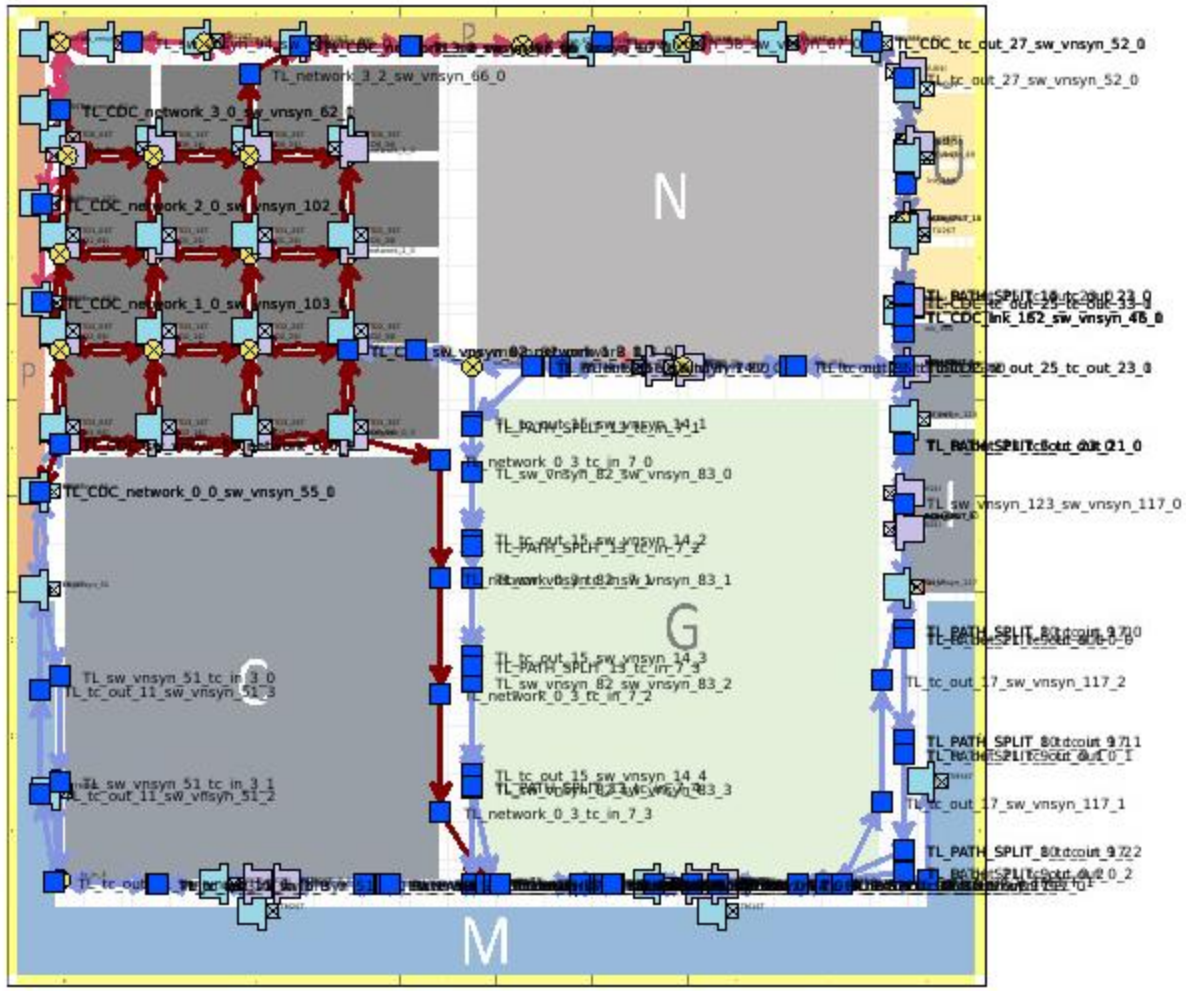
Step 3 Architecture level Timing closure

Insert the distance pipeline(s)







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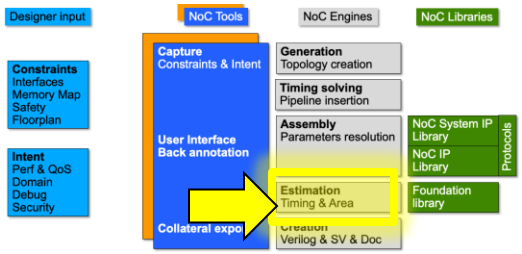
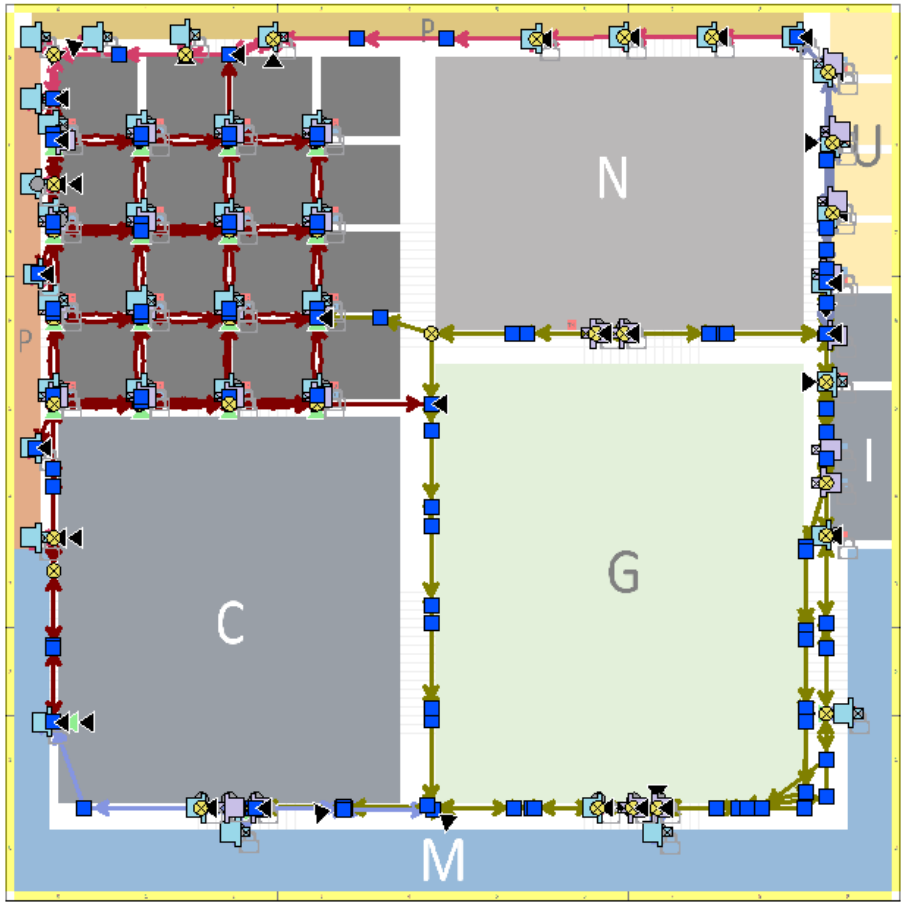
Step 3 Architecture level Timing closure

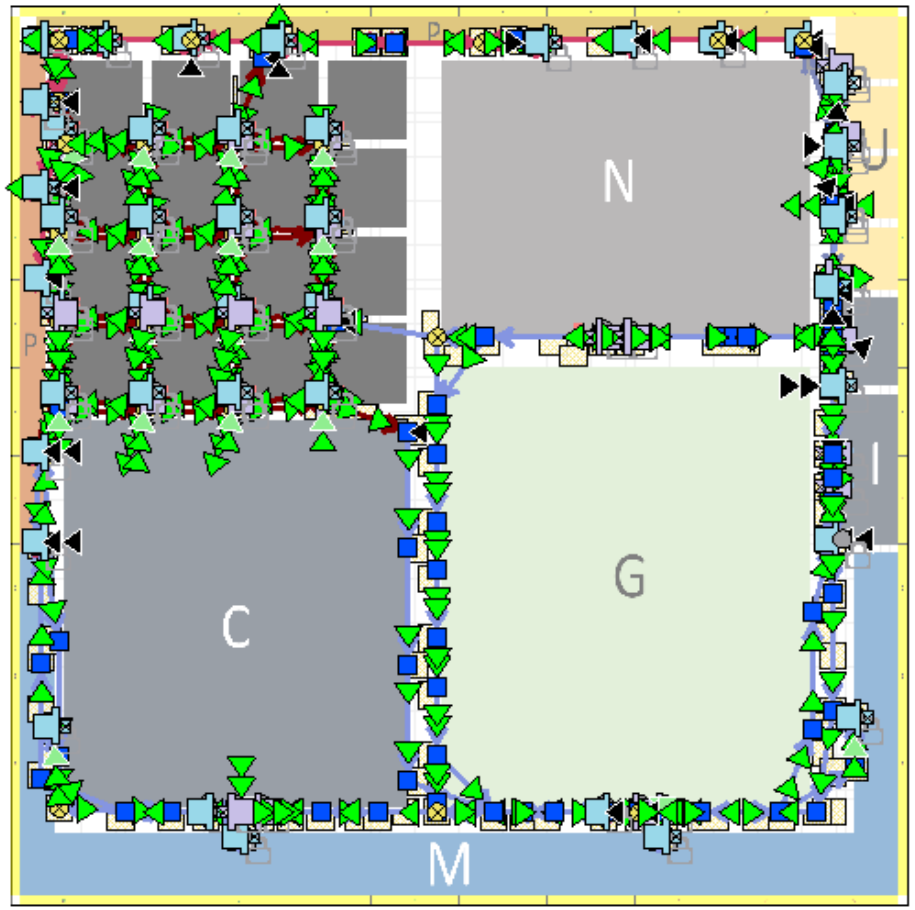
Results



Before

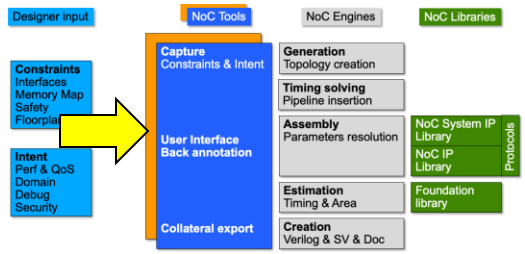


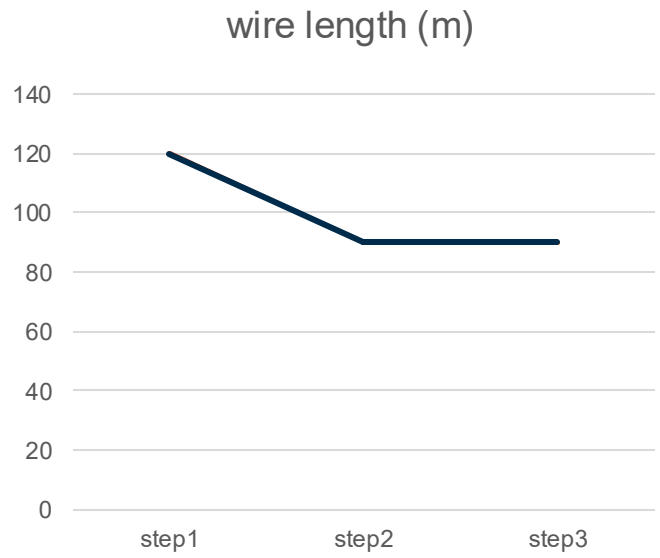
After



Step 3 Reverify Performance of Optimized NoC

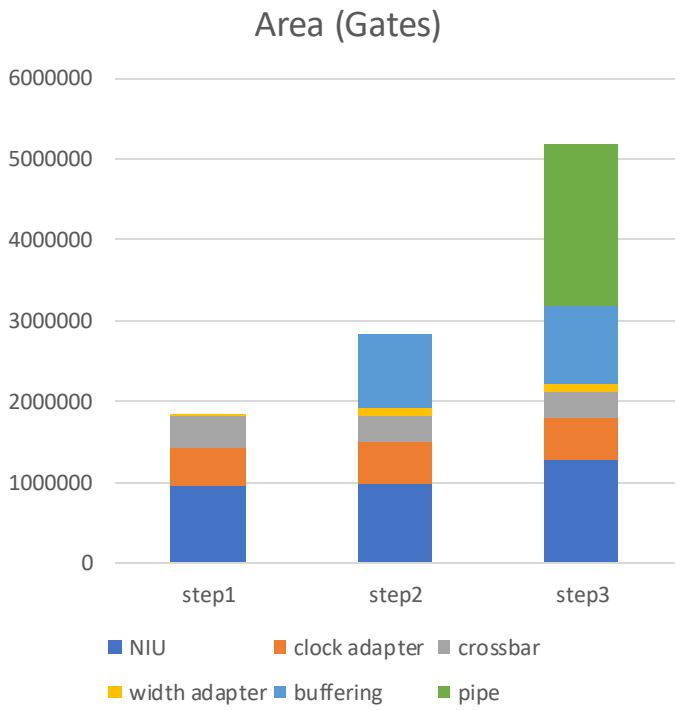
Re-run simulation scenario on architectural model





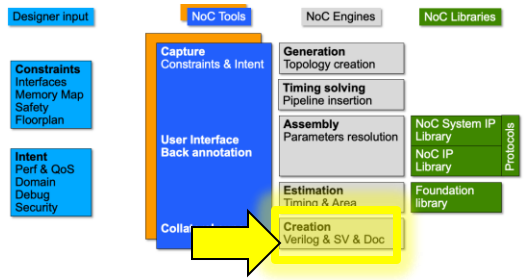
Row	Required Effic	Efficiency	Satisfaction	Through
P_ID1_0	90.0 %	98.6 %	PASS	6.9 GB/s
P_ID1_1	90.0 %	99.8 %	PASS	7.0 GB/s
P_ID1_2	90.0 %	100.0 %	PASS	7.0 GB/s
P_ID1_3	90.0 %	100.0 %	PASS	7.0 GB/s
P_ID2_0	90.0 %	99.8 %	PASS	7.0 GB/s
P_ID2_1	90.0 %	100.0 %	PASS	7.0 GB/s
P_ID2_2	90.0 %	100.0 %	PASS	7.0 GB/s
P_ID2_3	90.0 %	100.0 %	PASS	7.0 GB/s
P_ID3_0	90.0 %	100.0 %	PASS	7.0 GB/s
P_ID3_1	90.0 %	100.0 %	PASS	7.0 GB/s
P_ID3_2	90.0 %	100.0 %	PASS	7.0 GB/s
P_ID3_3	90.0 %	100.0 %	PASS	7.0 GB/s
P_IG0	90.0 %	100.0 %	PASS	6.0 GB/s
P_IG1	90.0 %	100.0 %	PASS	6.0 GB/s
P_II0	90.0 %	100.0 %	PASS	500.7 MB/s
P_II1	90.0 %	100.0 %	PASS	500.7 MB/s
P_II2	90.0 %	100.0 %	PASS	500.7 MB/s
P_IN0	90.0 %	100.0 %	PASS	6.0 GB/s
P_IN1	90.0 %	100.0 %	PASS	6.0 GB/s
P_IU0	90.0 %	100.0 %	PASS	2.0 GB/s
P_IU1	90.0 %	100.0 %	PASS	2.0 GB/s
P_IU2	90.0 %	100.0 %	PASS	2.0 GB/s
P_IU3	90.0 %	100.0 %	PASS	2.0 GB/s

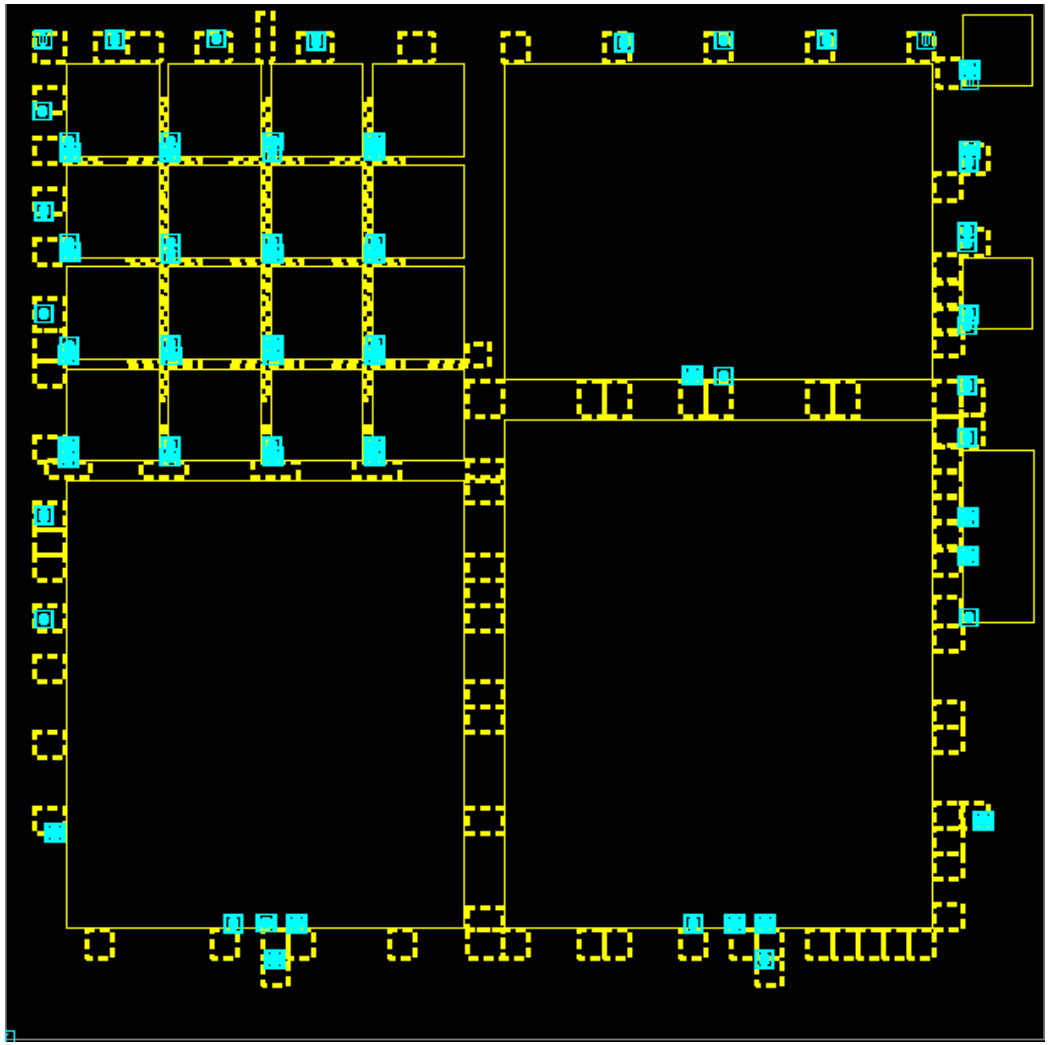
Row	Throughput	state
SLAVE_TD0_0_T_0	7.1 GB/s	
SLAVE_TD0_1_T_0	6.9 GB/s	
SLAVE_TD0_2_T_0	7.0 GB/s	
SLAVE_TD0_3_T_0	6.9 GB/s	
SLAVE_TD1_0_T_0	7.0 GB/s	
SLAVE_TD1_1_T_0	6.8 GB/s	
SLAVE_TD1_2_T_0	7.0 GB/s	
SLAVE_TD1_3_T_0	7.0 GB/s	
SLAVE_TD2_0_T_0	6.9 GB/s	
SLAVE_TD2_1_T_0	6.7 GB/s	
SLAVE_TD2_2_T_0	6.8 GB/s	
SLAVE_TD2_3_T_0	7.0 GB/s	
SLAVE_TD3_0_T_0	6.8 GB/s	
SLAVE_TD3_1_T_0	6.9 GB/s	
SLAVE_TD3_2_T_0	6.9 GB/s	
SLAVE_TD3_3_T_0	7.2 GB/s	
SLAVE_TM0_T_0	12.4 GB/s	
SLAVE_TM1_T_0	12.3 GB/s	
SLAVE_TM2_T_0	12.2 GB/s	
SLAVE_TM3_T_0	12.4 GB/s	

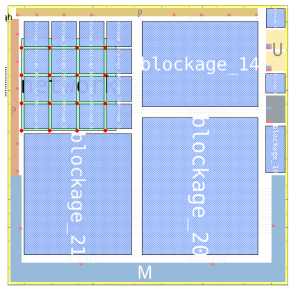


Step 4 Export for Physical Synthesis

Virtual floorplan for the Network-on-Chip is automatically generated





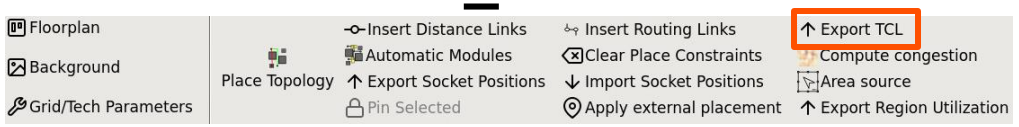


+

```
 62 ID3_1 1615.0
5734.000000000001
 63 TP13 3052.0 9831.0
 64 TP12 2068.0 9851.0
 65 TP11 1067.0 9842.0
 66 TP10 362.00000000000006
9847.0
 67 TP17 9035.0 9832.0
 68 TP16 8057.0 9842.0
 69 TP15 7054.000000000001
9833.0
 70 TP14 6065.0 9810.0
```

+

=




```
...
set_port_location TI1_HWrite -coordinate {9464.10500 4156.72800}
set_port_location TI1_HBurst[0] -coordinate {9466.17500 4156.72800}
set_port_location TI1_HBurst[1] -coordinate {9468.24500 4156.72800}
set_port_location TI1_HBurst[2] -coordinate {9453.75500 4157.30400}
set_port_location TI1_HSel -coordinate {9455.82500 4157.30400}
set_port_location RstN -coordinate {9457.89500 4157.30400}
set_port_location RegimeI_clk -coordinate {9459.96500 4157.30400}
set_port_location RegimeM_clk -coordinate {2228.89500 1144.30400}
set_port_location tm -coordinate {-3.10485 -0.28580}
set_port_location RegimeU_clk -coordinate {9452.38500 7955.03200}
set_port_location RegimeP_clk -coordinate {6061.89500 9812.30400}
set_port_location RegimeG_clk -coordinate {7173.38500 1142.03200}
set_port_location RegimeN_clk -coordinate {7061.38500 6535.03200}
set_port_location RegimeD_clk -coordinate {596.58000 5840.03200}
...
```


ARTERIS IP

Step 4 Check results of Physical Synthesis

Area Results, Architecture Area estimation was 98% Accurate

```
[gbaillieu@dell001srv sko2024FlexGenDemo]$ head -3 results_dir/Step8/bigDemoSpec.arch.Structure.area
                                  Instance                                  Total (NAND2X1) Comb (NAND2X1)  Dffs    %
-------------------------------------------------------------------------------- -------------- ------------- ------ ------
/bigDemoSpec.arch.Structure                                                 5197665        1507615        527150 100.00
```

```
****************************************
Report : area
Design : bigDemoSpec_arch_Structure
Version: R-2020.09-SP1
Date   : Tue Feb 27 18:43:54 2024
****************************************

Library(s) Used:

    sc10p5mcpp84_14lpp_base_rvt_c14_ssa_sigcmax_max_0p
/engr/dev/tools/techno/library/arm/samsung/14lpp/sc10p
    sc10p5mcpp84_14lpp_base_lvt_c14_ssa_sigcmax_max_0p
/engr/dev/tools/techno/library/arm/samsung/14lpp/sc10p
    sc10p5mcpp84_14lpp_base_slvt_c14_ssa_sigcmax_max_0
/engr/dev/tools/techno/library/arm/samsung/14lpp/sc10p

Number of ports:                      1841689
Number of nets:                       3402845
Number of cells:                      1599565
Number of combinational cells:        1056052
Number of sequential cells:            524064
Number of macros/black boxes:               0
Number of buf/inv:                     331615
Number of references:                     562

Combinational area:             275255.802532
Buf/Inv area:                    64844.472075
Noncombinational area:          593359.198829
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (Wire load has

Total cell area:                868615.001361
Total area:                 undefined
1
```

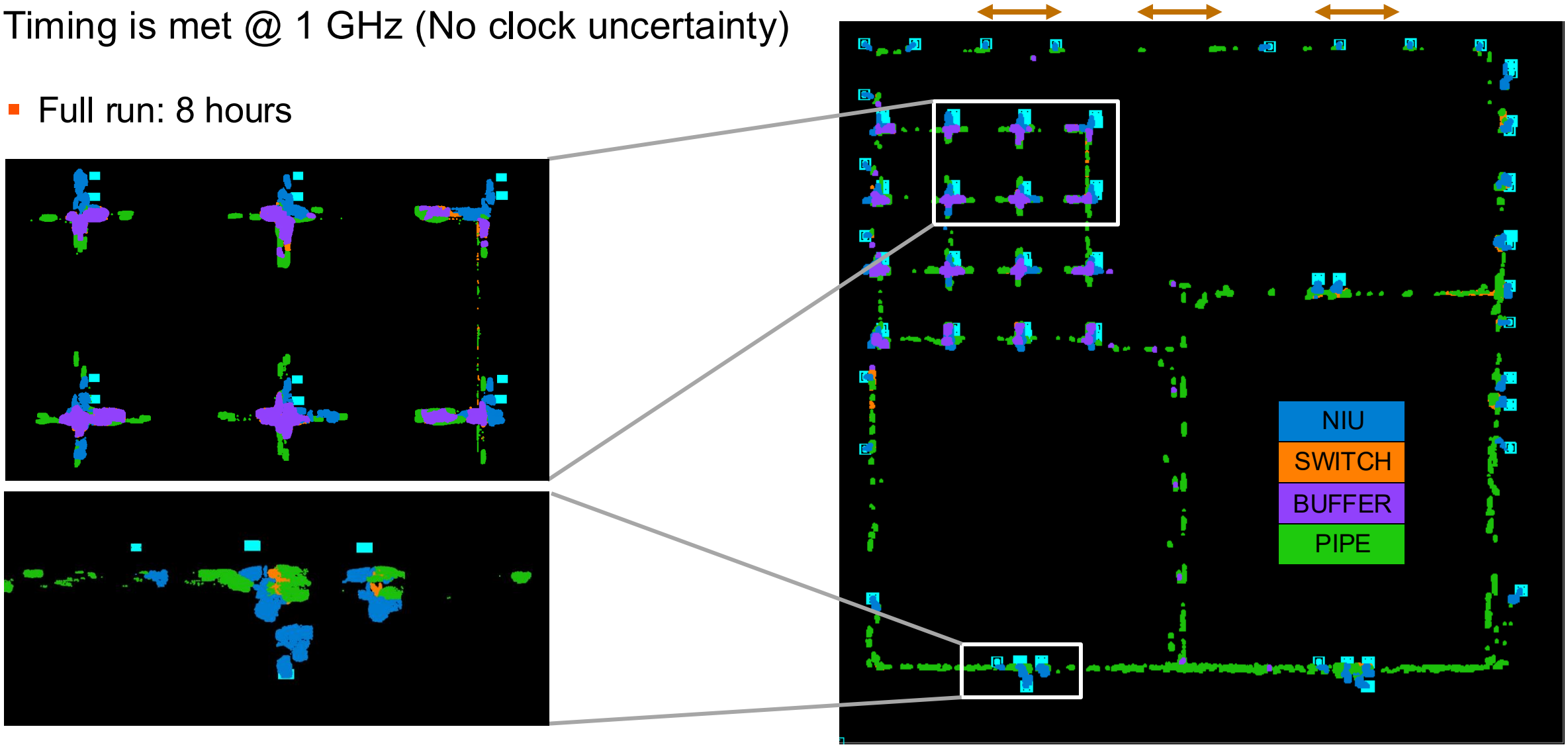
```
 ---------------------------------------- ---------------------- ------------------- ------------------------ -------------------------
 Library cell distribution                 Total (um2)      (%)     Comb (um2)    (%)      Dffs (um2)    (%) (nb)     ICG (um2)     (%) (nb)
---------------------------------------- ---------------------- ------------------- ------------------------ -------------------------
sc10p5mcpp84_14lpp_base_lvt_c14_ssa_sigcmax_max_0p72v_125c   16701.72 (  1.92)       5848.75 ( 0.67)       9867.28 ( 1.14) ( 8602)     985.69 ( 0.11) (  521)
sc10p5mcpp84_14lpp_base_rvt_c14_ssa_sigcmax_max_0p72v_125c  841577.87 ( 96.89)     269407.06 (31.02)     568699.83 (65.47) (503860)    3470.99 ( 0.40) ( 4074)
sc10p5mcpp84_14lpp_base_slvt_c14_ssa_sigcmax_max_0p72v_125c   10335.40 (  1.19)          0.00 ( 0.00)          0.00 ( 0.00) (    0)   10335.40 ( 1.19) ( 7007)

---------------------------------------- ---------------------- ------------------------ ------------------------ ------------------------ -------------------------
  Name Group filter                        Total (Kgate)     (%)    Comb (Kgate)   (%) (nb)   Buf/inv (Kgate) (%) (nb)   Dffs (Kgate)    (%) (nb)     ICG (Kgate)     (%) (nb)
---------------------------------------- ---------------------- ------------------------ ------------------------ ------------------------ -------------------------
GenericToTransport                          495.32 (  9.00)      152.17 ( 2.00) (95404)       64.03 ( 1.00) (56219)      257.45 ( 5.00) (38761)       21.67 ( 0.00) ( 4150)
TransportToGeneric                          165.10 (  3.00)       30.57 ( 0.00) (18401)       45.74 ( 0.00) (35698)       85.43 ( 1.00) (12817)        3.37 ( 0.00) (  542)
SpecificToGeneric                           168.57 (  3.00)       33.75 ( 0.00) (18173)        2.12 ( 0.00) ( 2640)      130.11 ( 2.00) (19517)        2.59 ( 0.00) (  324)
GenericToSpecific                           142.50 (  2.00)       34.92 ( 0.00) (20951)        3.21 ( 0.00) ( 4350)      101.75 ( 1.00) (15260)        2.62 ( 0.00) (  392)
Clock_adaptation                            442.54 (  8.00)       59.07 ( 1.00) (37302)       18.69 ( 0.00) (15467)      356.75 ( 6.00) (53564)        8.04 ( 0.00) (  858)
PowerDisc                                     0.00 (  0.00)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)
Pipe_Transport                             2037.92 ( 39.00)      264.20 ( 5.00) (115893)      128.80 ( 2.00) (95002)     1617.56 (31.00) (242419)       27.36 ( 0.00) ( 2922)
Generic_Pipe                                153.78 (  2.00)       18.09 ( 0.00) ( 8001)        6.75 ( 0.00) ( 5482)      126.94 ( 2.00) (19033)        2.00 ( 0.00) (  207)
Mux_and_Demux                               371.67 (  7.00)      301.74 ( 5.00) (227072)       48.68 ( 0.00) (58696)       20.01 ( 0.00) ( 2999)        1.24 ( 0.00) (  245)
Width_conversion                            109.31 (  2.00)       38.26 ( 0.00) (23720)        8.22 ( 0.00) ( 7725)       61.27 ( 1.00) ( 9202)        1.56 ( 0.00) (  228)
buffering                                    41.09 (  0.00)        9.37 ( 0.00) ( 5005)        1.04 ( 0.00) (  978)       30.06 ( 0.00) ( 4509)        0.63 ( 0.00) (   80)
Memory_Scheduler                              0.00 (  0.00)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)
Reorder_Buffer                                0.00 (  0.00)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)
TimeOut                                       0.00 (  0.00)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)
Translation_Table                             3.37 (  0.00)        2.22 ( 0.00) ( 1517)        1.15 ( 0.00) ( 1547)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)
Mode_Decode                                   0.00 (  0.00)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)
ErrorLog                                      0.00 (  0.00)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)
SidebandManager                               0.00 (  0.00)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)
ClockManager                                  0.29 (  0.00)        0.00 ( 0.00) (    0)        0.19 ( 0.00) (  112)        0.10 ( 0.00) (   14)        0.00 ( 0.00) (    0)
ClockGater                                   25.60 (  0.00)        2.00 ( 0.00) ( 1478)        8.04 ( 0.00) ( 5869)        9.90 ( 0.00) ( 1485)        5.66 ( 0.00) (  495)
Firewall                                      0.00 (  0.00)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)
QoS                                           0.00 (  0.00)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)
Probe                                         0.00 (  0.00)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)
STPv2Converter                                0.00 (  0.00)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)
PowerControl                                  0.00 (  0.00)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)        0.00 ( 0.00) (    0)
others                                      972.24 ( 18.00)      296.16 ( 5.00) (151520)       46.27 ( 0.00) (41830)      619.20 (12.00) (92882)       10.62 ( 0.00) ( 1159)
---------------------------------------- ---------------------- ------------------------ ------------------------ ------------------------ -------------------------
Total                                      5129.29 (100.00)     1242.51 (24.00) (724437)      382.92 ( 7.00) (331615)     3416.52 (66.00) (512462)       87.35 ( 1.00) (11602)
```

Step 4 Smart NoC-Driven Physical Synthesis

Timing is met @ 1 GHz (No clock uncertainty)

- Full run: 8 hours

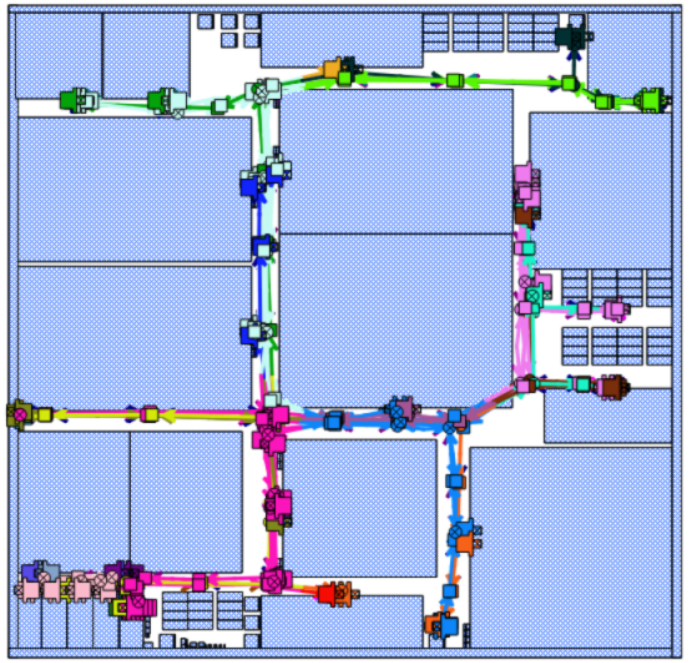


Use Cases

Sample Results for Automotive AI SoC (ADAS)

DREAM CHIP

Manual

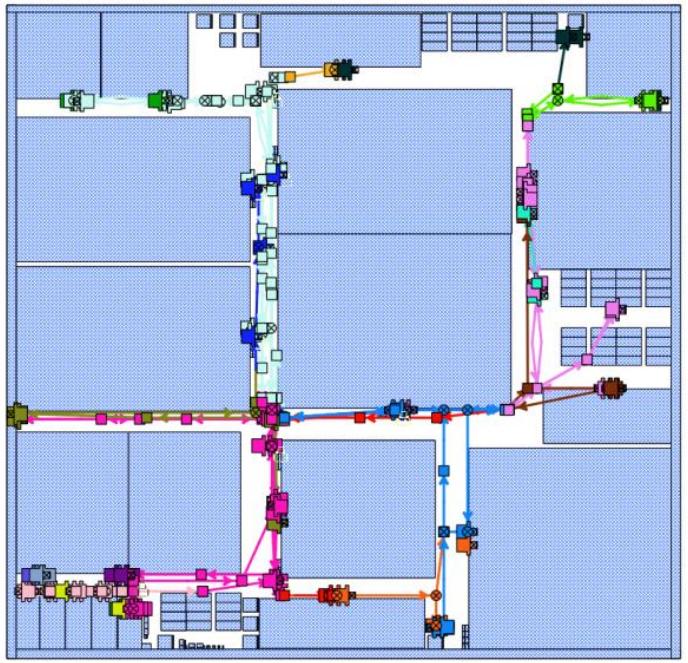


Total Wire Length	138,709 mm
Length of Longest Wire	904 mm
Number of Switches	258
Number of Links	313
No. of Clock Adapters	152
No. Packet Adapters	157
Latency	65.18 ns
Maximum Latency	1005.67 ns
Main NoC area	3.64 mm^2

10x productivity
-26% wire length
-28% longest wire

-5% latency
-51% max latency
-3% area

Smart NoC Automated



Total Wire Length	102,587 mm
Length of Longest Wire	650 mm
Number of Switches	282
Number of Links	420
No. of Clock Adapters	141
No. Packet Adapters	210
Latency	62.08 ns
Maximum Latency	491.67 ns
Main NoC area	3.51 mm^2

ARTERIS IP

Similar Results Seen Across Many Applications

Use Case	Manual (NoC Expert)	Automated (Smart NoC)	Productivity Gain
AI SoC	20 hours	2 hours	10x

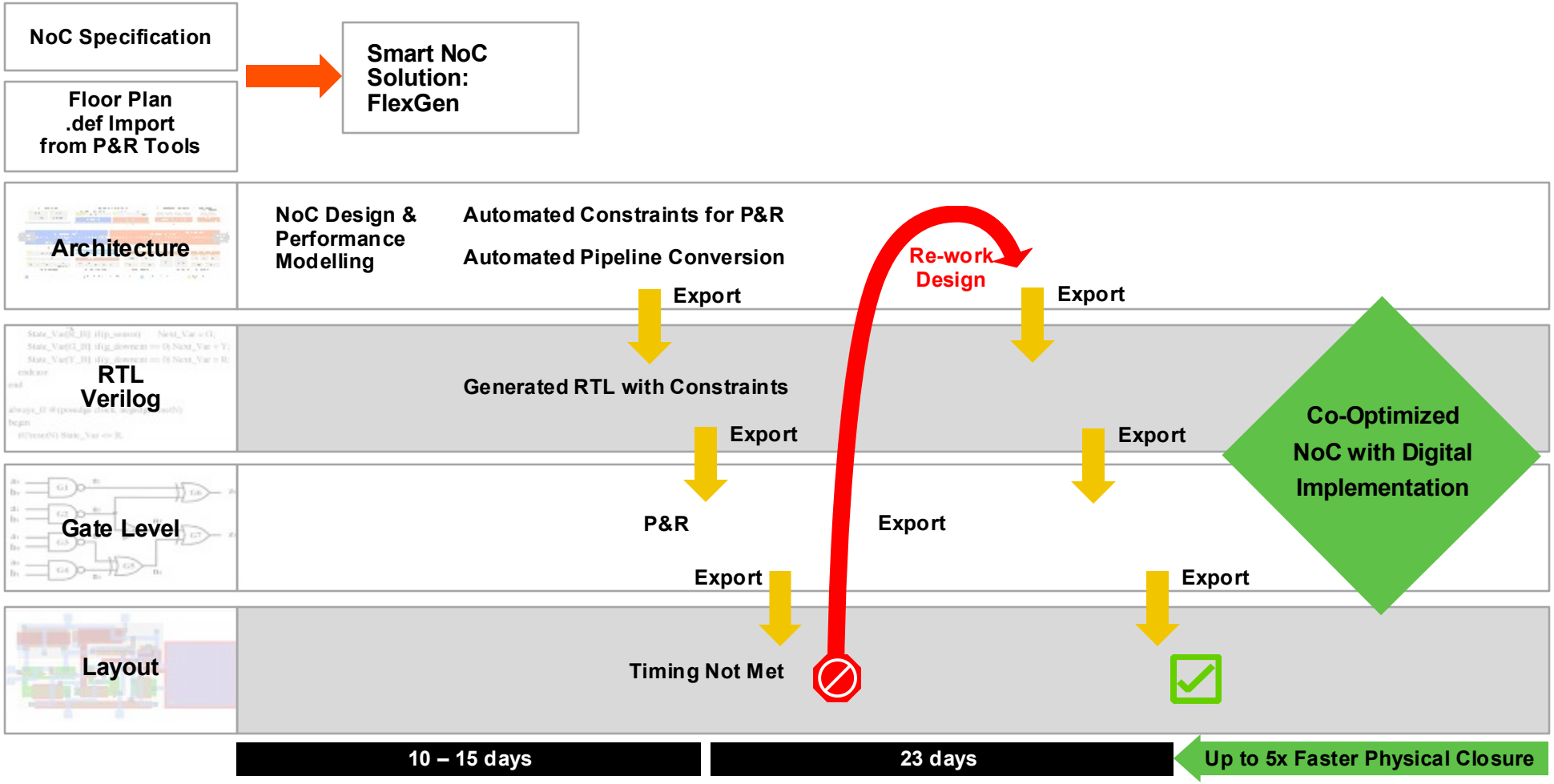
Use Case	Manual (NoC Expert)	Automated (Smart NoC)	Productivity Gain
ADAS SoC	24 hours	2.5 hours	9.6x

Use Case	Manual (NoC Expert)	Automated (Smart NoC)	Productivity Gain
SSD Controller SoC	30 hours	2.5 hours	12x

ARTERIS IP

Accelerating SoC Design

Avoiding late timing issues using abstraction, physical awareness, and estimation

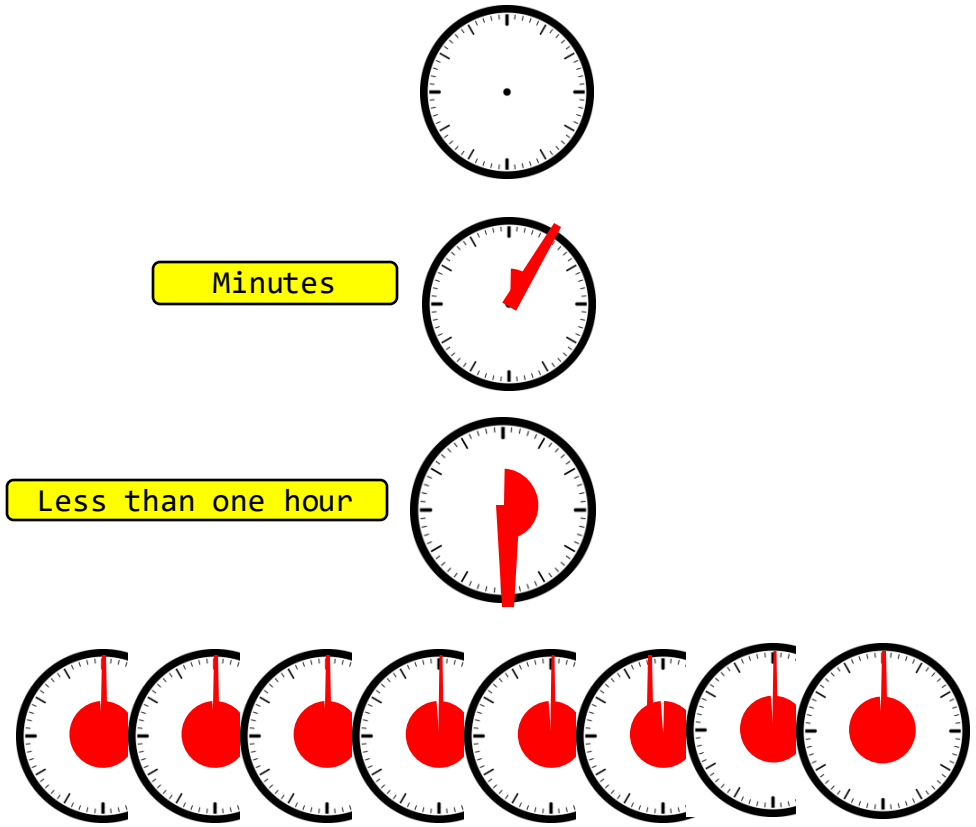


ARTERIS IP

Conclusion

Reduced Turnaround Time Compared To Manual NoC Generation

Incremental change turn-around time



Smart NoC Flow (Arteris FlexGen)

Step 1
- Create a Network-on-Chip **specification**
- Assign initial high-level performance parameters
- **Verify performance** with architectural model and simulation

Step 2
- Capture virtual **floor planning** constraints and specify **performance intent**
- **Smart NoC** generates Network-on-Chip topology
- **Verify performance** with architectural model and simulation

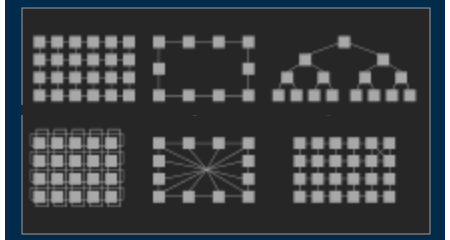
Step 3
- Insert **pipeline** slice with built in Static Timing Analysis (STA) engine
- **Verify performance** with architectural model and simulation

Step 4
- Create a physical synthesis **framework**
- Validate with physical synthesis tools using Smart NoC **constraints**

Arteris – Addresses Emerging Trends in Electronics

Growing design complexity, tightening performance constraints and lack of NoC expertise compound time-to-revenue challenges

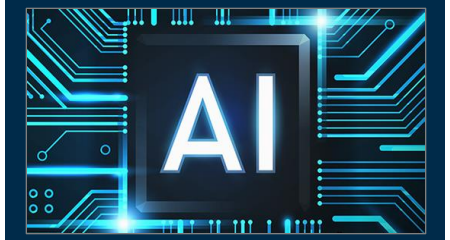
Accelerating Complexity



More Processors & IP Blocks Data movement key competency ‘Data movement and storage operations can account for up to 84% of the dynamic energy usage of a GPU's system-on-chip (SoC)*.’

*Source: HAL open science paper, Jun’24

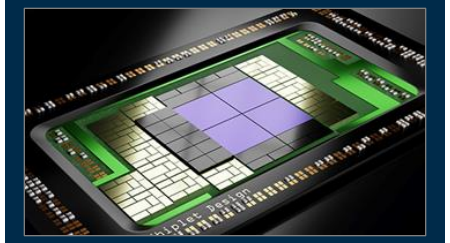
Artificial Intelligence



By 2030, the total generative AI compute will serve 70 percent of business-to-consumer and 30 percent of business-to-business applications **.’

**Source: McKinsey, Mar’24

Chiplets



‘Multi-die systems have emerged as the solution to go beyond Moore’s law and address the challenges of systemic complexity***.’

***Source: Semiconductor Engineering Oct’23

OEMs Going Vertical

‘OEMs are increasingly embracing vertical integration in their design practices, including implementing their own SoCs.****.’

****Source: Synopsys Feb’22

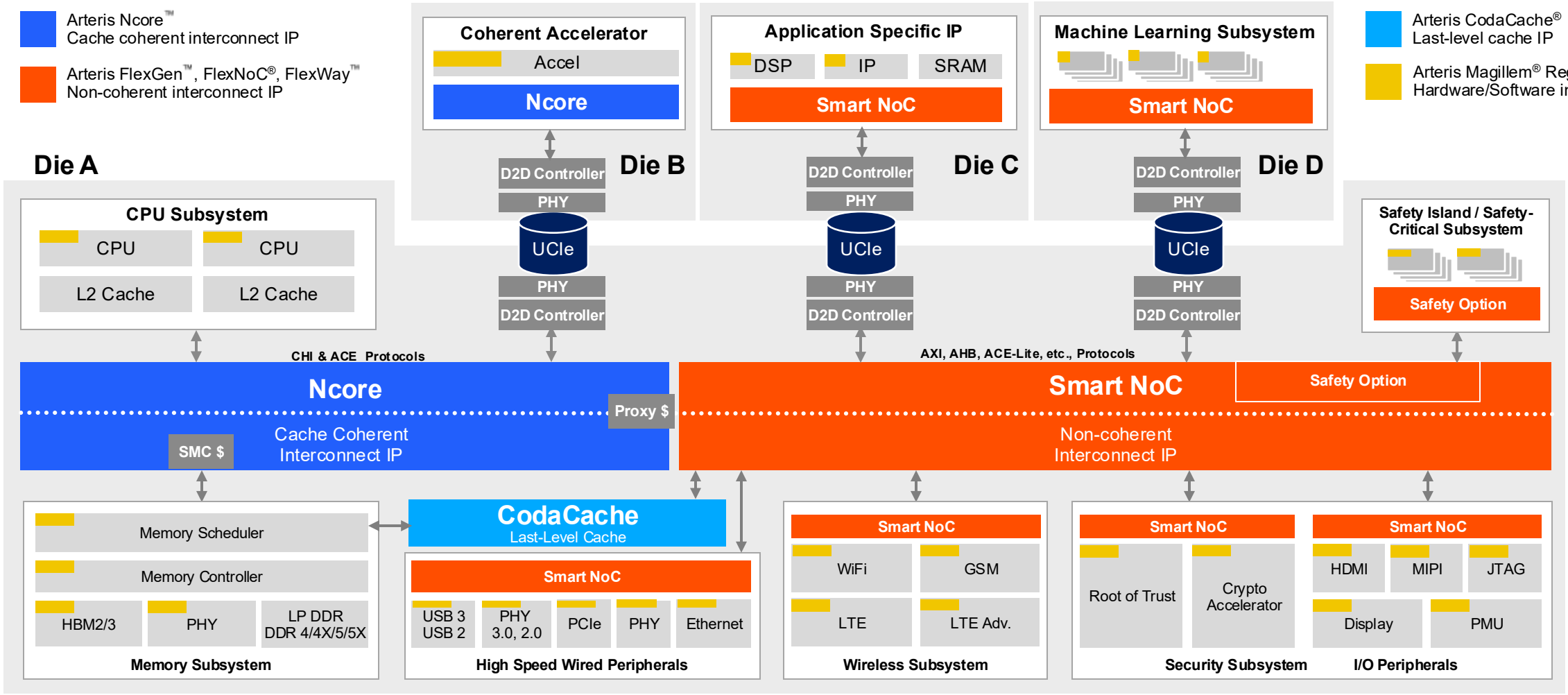
Robotics

‘Humans are set to interact with polyfunctional robots at an increasing rate: 80% of us will use them on a daily basis by 2030, up from 10% today*****.’

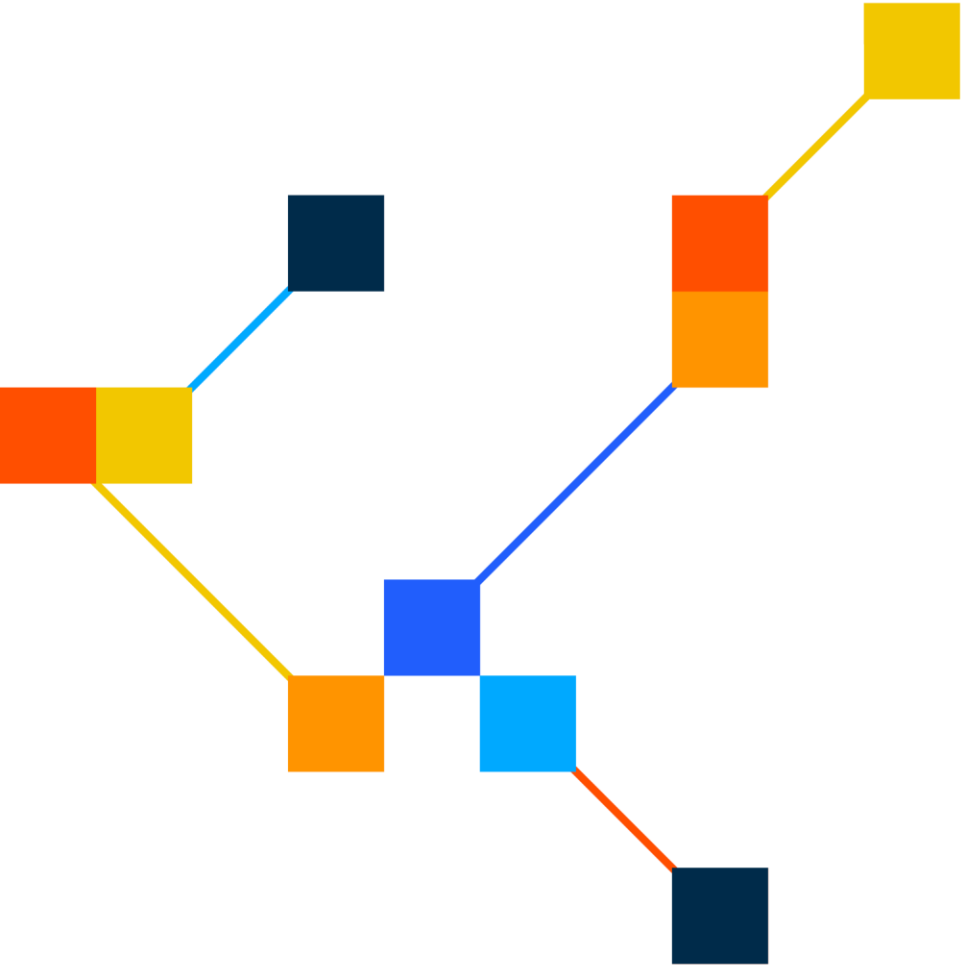
*****Source: Forbes Oct `24

Multi-Die System IP and Network-on-Chip (NoC) SoC Interconnect IPs

Smaller Die Area | Lower Power Consumption | Faster Frequency Lower Latency | Shorter, Predictable Schedules | Rapid Timing Closure Estimation | Automated Verification | Easy Configuration



ARTERIS IP



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Thank you

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