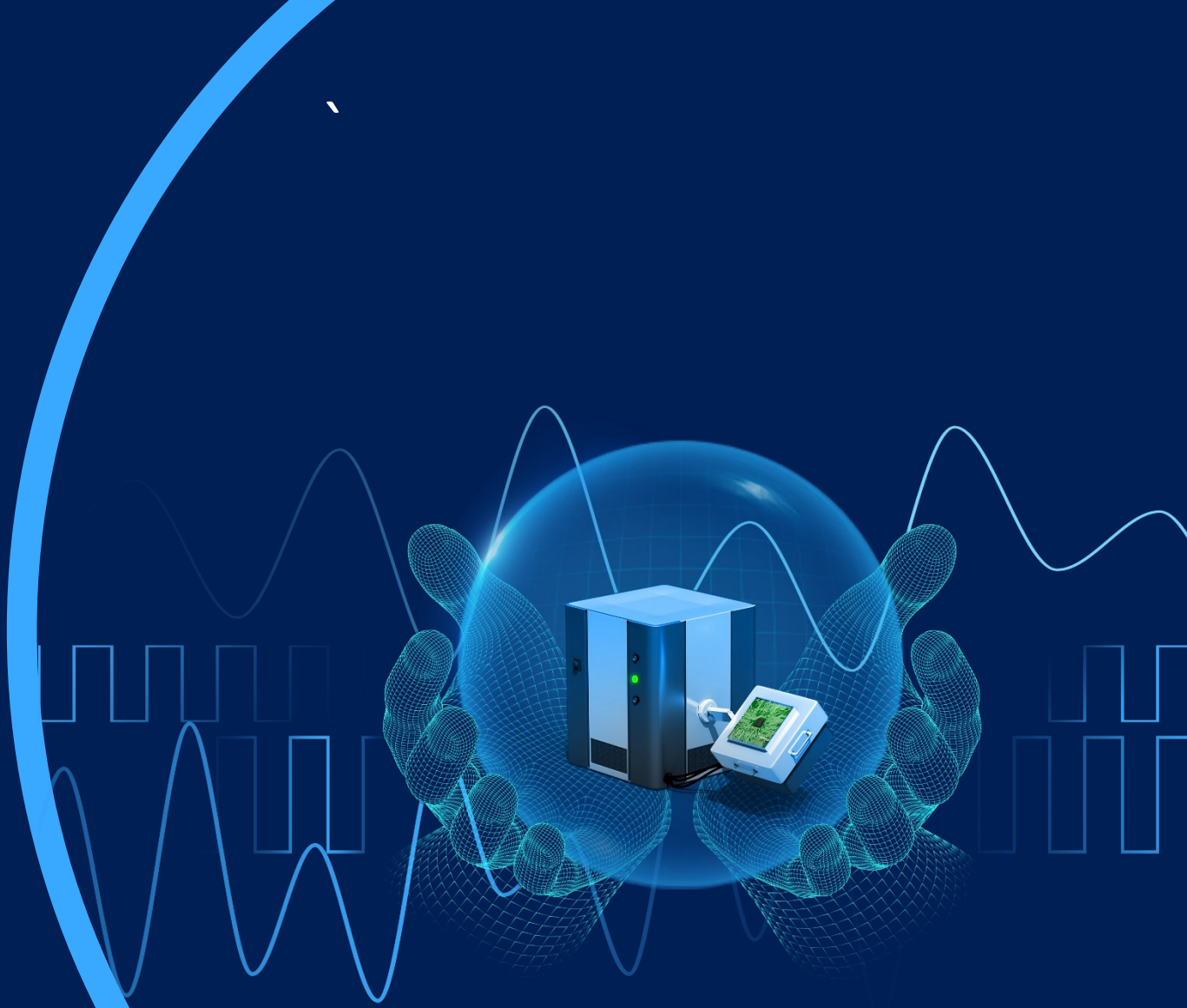
testinsight
LINKING DESIGN & TEST

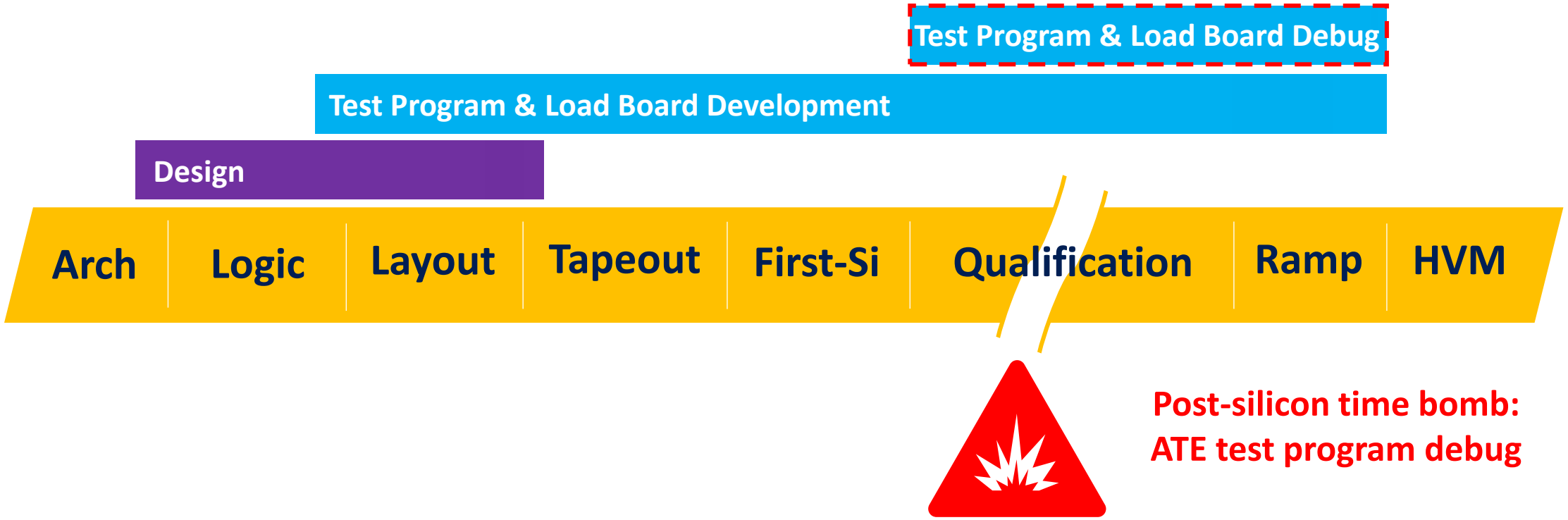
Get Ready for Production Test Before Silicon With an ATE Digital Twin



Skip intro

Challenge: Late Test Program & Load Board Validation

- Test program & load board debug starts only after first-si
- Although the test program can be ready long before TO
- Potential delay in HVM & sample delivery to customers



Why Test Program Validation by EDA Is Not Enough

- EDA tools emulate the chip, ignoring ATE limitations
- Unaware of pattern conversion to ATE format
- Limited coverage of complex elements, such as:
  - 3rd party IP integration (SERDES, PCIe, etc.)
  - Multi-core dies
  - Multi-die packages
  - Focus only on the model upon ATE failures

The Desired Solution: Pre-silicon Validation

- Debug the test program & load board before silicon arrives

What if You Had an ATE Digital Twin?

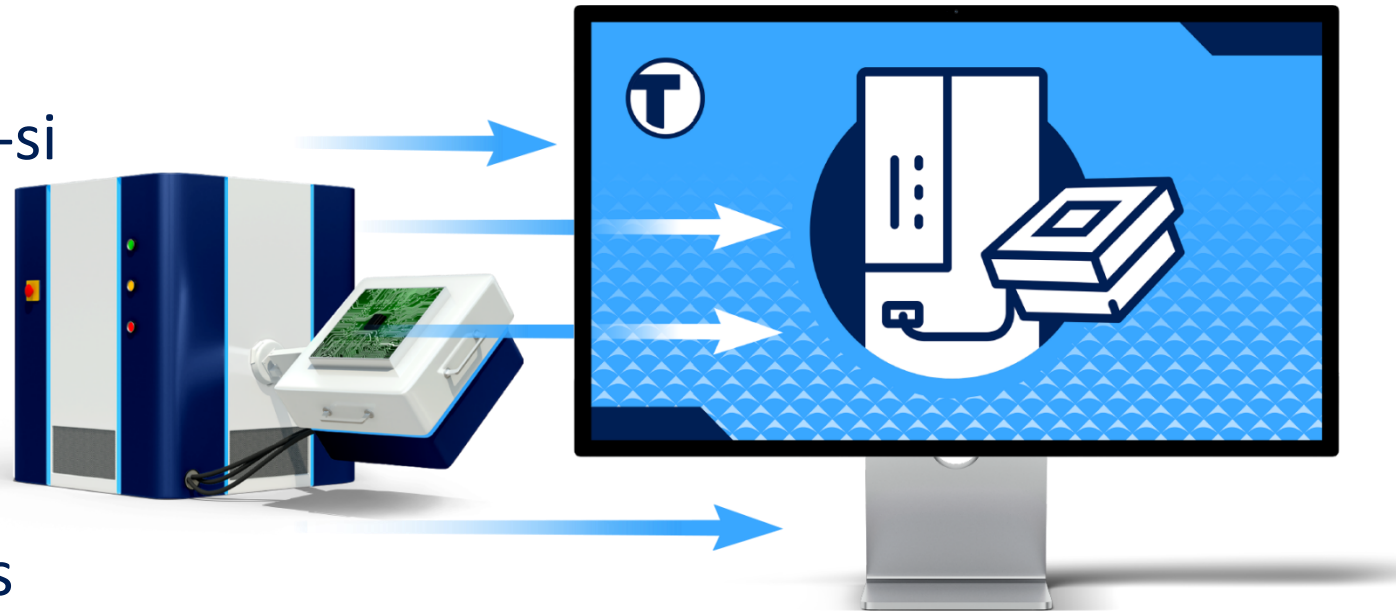
- Emulate the ATE tester
- Predict post-si test results
- Debug faster using EDA tools
- Verify your test program pre-si
- Validate load board design pre-si

No avoidable re-spins

No excessive tester time

No preventable customer returns

No whopping production test costs



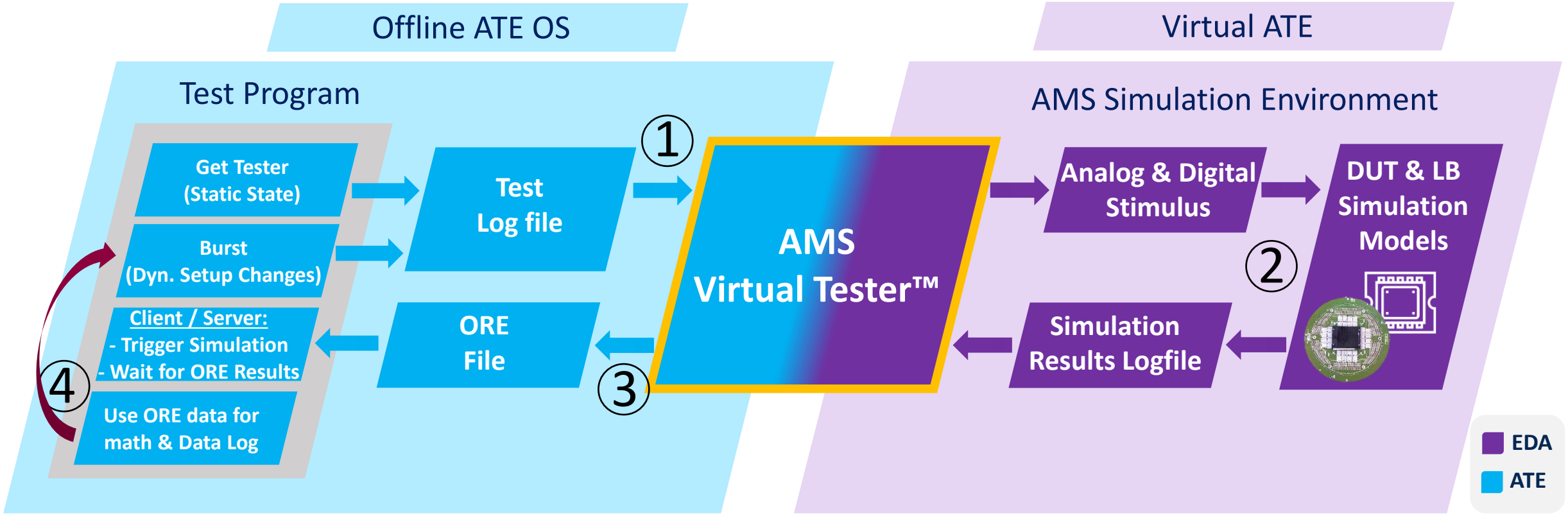
Gain Confidence in Your Test Program & Load Board Before Tapeout!

Virtual Tester™: Plan For Production Test Now

- Simulate the tester and test program with a model of the DUT
- Seamlessly Switch Between Simulation & Production
- Prepare in advance for the tester environment
- Gain confidence in your test program and load board design
- Improve the chances of tests working the first time

Release Your Test Program in Days vs. Weeks/Months

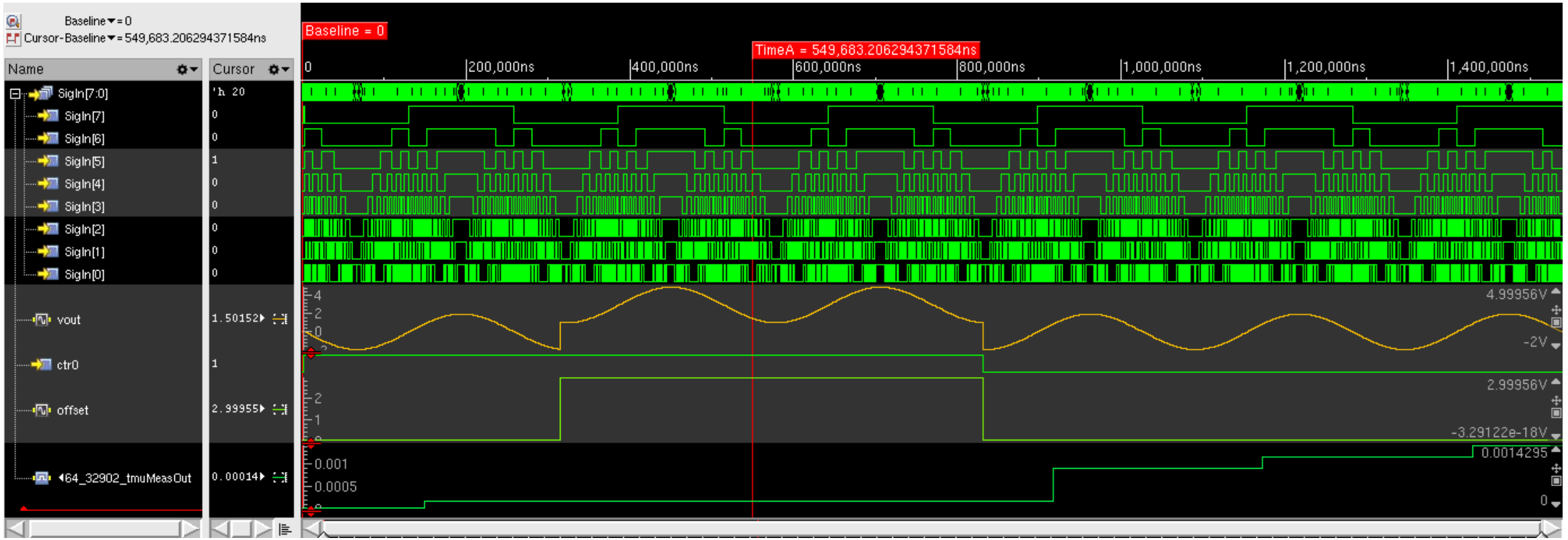
How Virtual Tester Works



1. AMS-VT records all test activity using Test log file
4. The offline ATE OS emulates the test program flow

2. Emulating ATE operations such as:
   - AC/DC stimulus driving DUT signals
   - Measure voltage/current on DUT signals
   - Measure timing/Freq of DUT signals etc'
3. Results are sent back to the ATE OS

Viewing Measurement Points in SimVision



What You Can Verify & Debug With AMS-VT

- **Test program** flow, test result manipulation, and pass/fail states.
- **ATE instruments** & **DUT setup** throughout the test execution.
- **ATE-DUT connectivity** at every stage of the test program.
- **Load board** programmable elements state e.g. relays.
- **Sync digital** patterns & **analog** portions of the test.

Ensure That All Parts Are in Sync: Test Program, ATE, DUT & Load Board

FAQ (1)

How do I get the load board model?

Standard PCB design tools like Cadence Allegro can dump a Verilog netlist

What Is Required To Run AMS-VT?

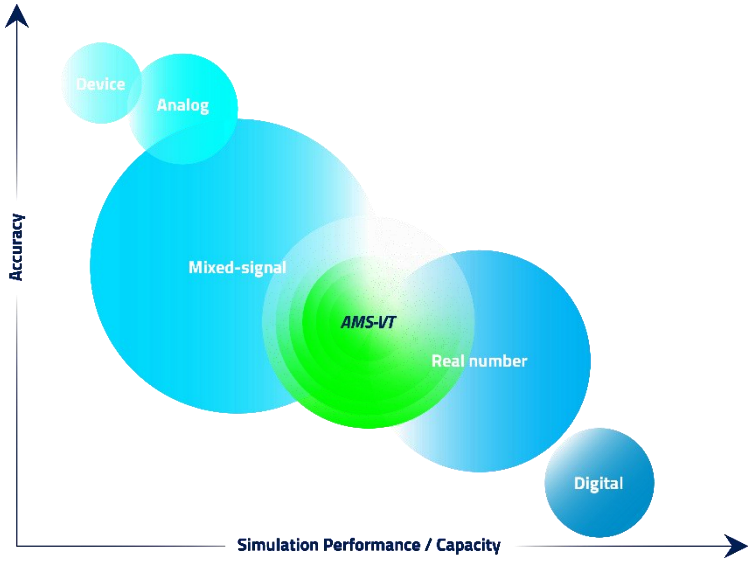
- DUT & load board models
- Working test program
- EDA environment
- Offline ATE OS
- ATE OS Log file and ORE

FAQ (2)

What Is the Effect on Simulation Time When Using AMS-VT?

- Overall runtime depends mainly on your DUT simulation time
  - AMS-VT Adds a few percentages of runtime.
  - Example: AMS-VT ran 25,000 tests of a modern mixed-signal production SoC in ~45 minutes.
- AMS-VT uses behavioral modeling instead of SPICE to keep runtime short
  - High-level DUT models are sufficient for ATE test program verification (see here.)

Modeling approach	Simulation type	Modeling language
Device/Physical	Continuous	SPICE, Spectre
Analog	Continuous	Verilog-A
Mixed-Signal	Continuous/Discrete	Verilog-AMS, VHDL-AMS
Real number	Discrete	Verilog-AMS/wreal, VHDL, SystemVerilog/RNM
Digital/Logic	Discrete	Verilog, VHDL, SystemVerilog



The effect of AMS modeling on simulation times

Customer Case Studies - ATE Digital Twin (VT™)

Case #1 - WiFi Chipmaker
Commenced Production After a Major Setback

- Spent a week to debug a failure on ATE
- Delayed customer shipments
- VT identified the issue immediately
- Production commenced the next day
- Reducing about 90% of post-silicon debug
- Post-mortem analysis revealed:
  - A design-to-test compatibility issue: A signal with a nonexistent PU
  - The failure on ATE was inconsistent
  - The failure on VT simulation was consistent and easy to reproduce

Case #2 - Data Center Chipmaker
Slashed Silicon Bring-up From Months to Days

- Typically spent months on post-si debug
- Wanted to accelerate time-to-market
- Found gaps between Verilog simulations & Si
- Missing clocks/reset signals caused delays
- VT found critical errors missed by simulation
- Reducing about 95% of post-silicon debug
- Shipped samples to customers within one week instead of a few months

Shipping Samples to Customers in as Early As One Week Instead of a Few Months With VT

“we expect AMS-VT to significantly reduce our development time, leading to a shortened time-to-market of new products”

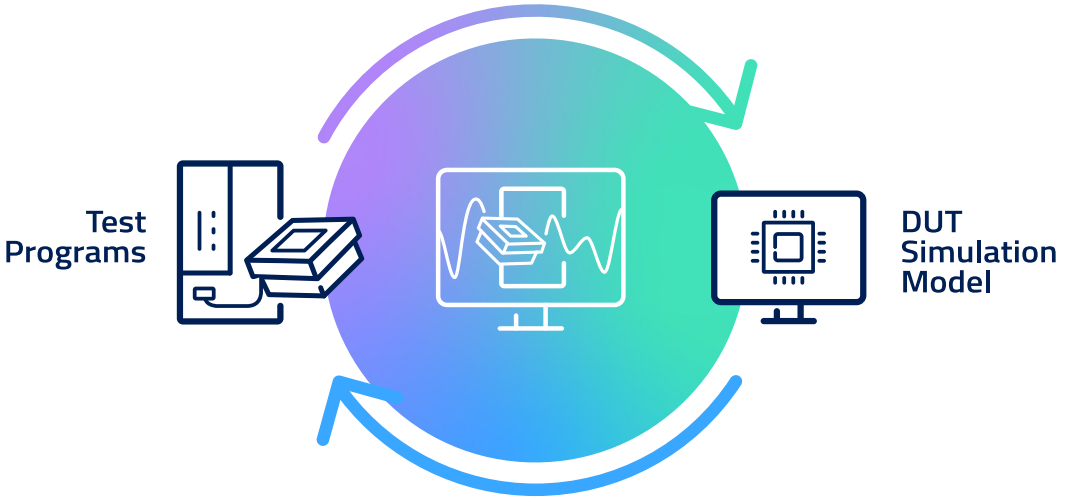
Even though AMS-VT is still being validated and integrated into NXP’s new-product-introduction process, we have already confirmed how powerful it can be. It has enabled us to perform early simulations with the entire tester setup, i.e., the device under test, the loadboard, and tester instruments, and thus obtain early knowledge of the product under development. Furthermore, we expect it to significantly reduce our development time, leading to a shortened time-to-market of new products. We are excited to see what NXP can achieve with this new tool.

Dr. ir. Guilherme Cardoso Medeiros

NXP

The ATE Digital Twin Opportunity

- Virtual Tester™ is the ATE digital twin
- Enable continuous test program enhancements
- Optimize the test program before Si!
- Provide test engineers with design insights
- Build a structured test development process
- Enable test program regression verification
- Linking Design & Test



Get Ready for Production Test Before Silicon With an ATE Digital Twin

Q&A

testinsight

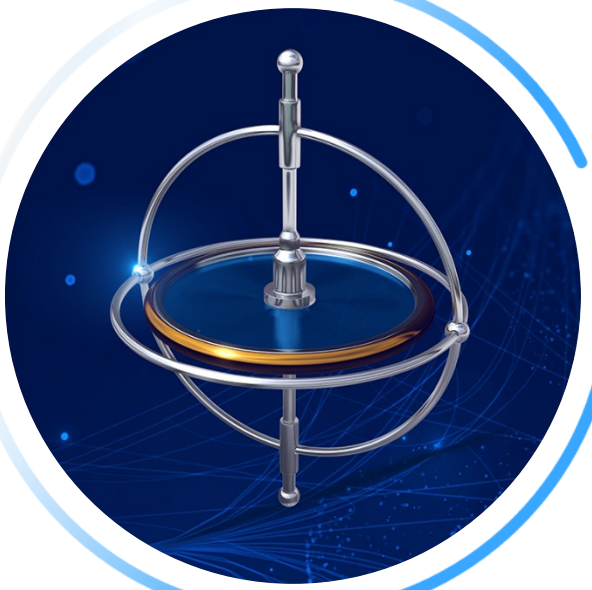
Questions?

AMS-VT™

MIXED-SIGNAL VIRTUAL ATE

GAIN CONFIDENCE IN YOUR 93K TEST PROGRAM AND LOAD BOARD DESIGN

Your Test Program at Its Best



Breakthrough ATE Digital Twin Technology

Accelerate Test Program Bring Up, Reduce Test Cost and Minimize Post-Silicon Debug

Up to 200x Faster ATE Software Tools

Getting You Faster to a High-Quality Test Program

Your Trusted ATE Software Partner

Trusted by Hundreds of Semiconductor Companies Worldwide Since 1999

TestInsight Summary

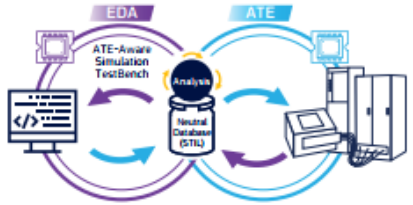
- Founded in 1999, privately held, continuously profitable
- Largest Design2Test company (R&D & Support)
- ADVANTEST® & TERADYNE OEM partner since 2001
- Local support offices worldwide

TestInsight Products

TDL Design2Test Conversion

Converting design vectors into ATE programs

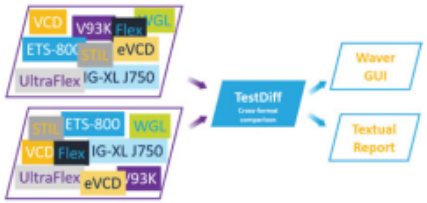
The proven fastest conversion tool on the market combines powerful innovation with ease of use and GUI, leading to faster high-quality test development



Virtual Tester (VT)

Pre-silicon test program validation

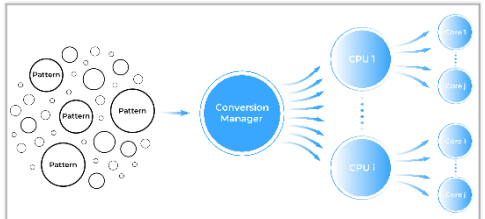
Creates an ATE-aware test bench, allowing pre-silicon testing with same results as post-silicon ATE, making production test debug shorter and more predictable



TestDiff

Cross-format test comparison

Compares test vectors of different EDA and ATE formats at waveform level for improved quality and debug flow, tracking down the root cause of any difference



Conversion Manager

Parallel Pattern Conversion Management

Accelerates test program bring-up by parallelizing incremental pattern conversion across multiple CPUs for greater efficiency.

AMS-VT

Analog/Mixed-Signal Virtual Tester

TestInsight's AMS Virtual ATE, allows you to debug your test program and load board before silicon arrives.

A Comprehensive Toolset for Linking Design and Test

A Few of Our Customers

Plus many others !

testinsight
LINKING DESIGN & TEST

Thank You!

www.testinsight.com