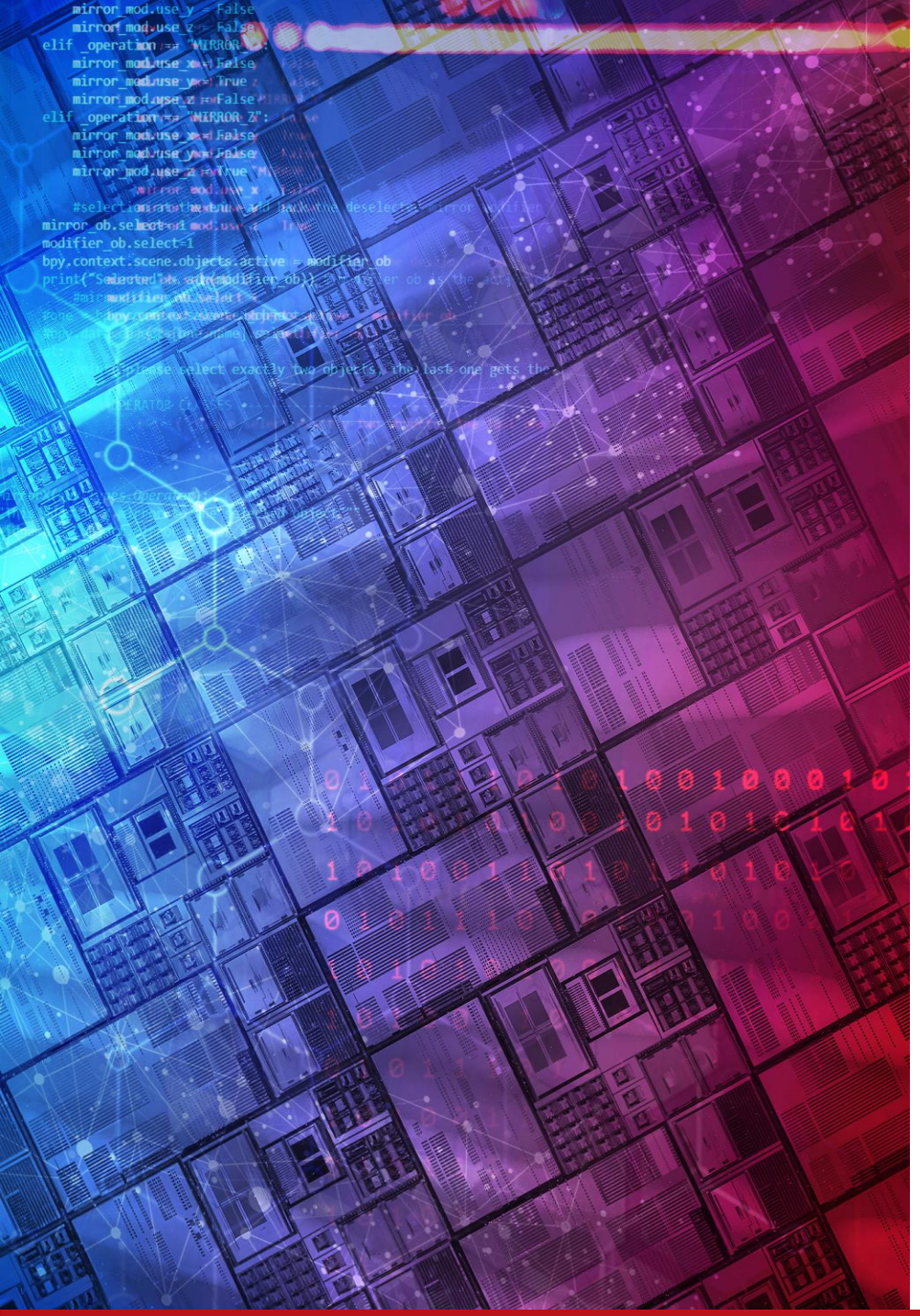

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SEMISRAEL 2025 EXPO

Booth #25

Automating the move to Advanced Technology Nodes

Andrew Patterson
Business Director, Silvaco EMEA

11th November 2025

Silvaco at a Glance

Silicon IP, and Management

Large portfolio: I3C, AMBA Fabric, MIPI PHYs, I/O, Memory Compilers, CAN/FD/XL/Automotive, Standard Cell Libraries, SRAM, IP Management Tools

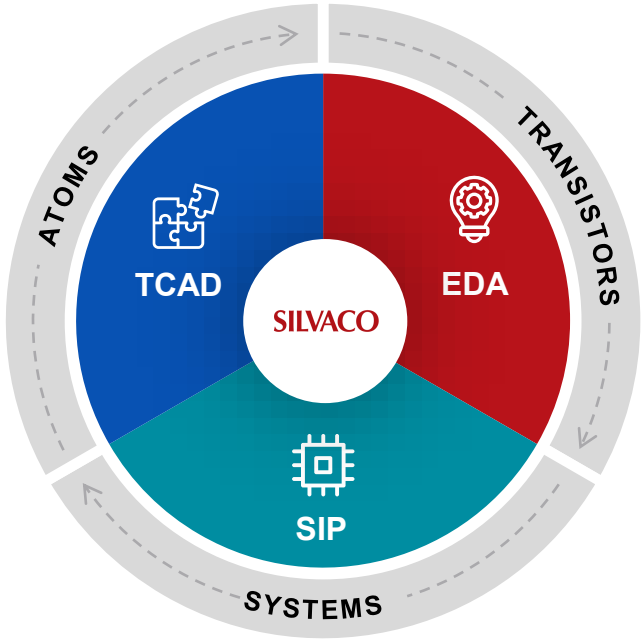
Leading TCAD Solution

Complete 2D/3D process, device modeling, simulation, power, photonics

EDA / IC Analysis & Verification Tools

Parasitic reduction and analysis, Variation analysis, Sign-off Verification

NASDAQ : SVCO



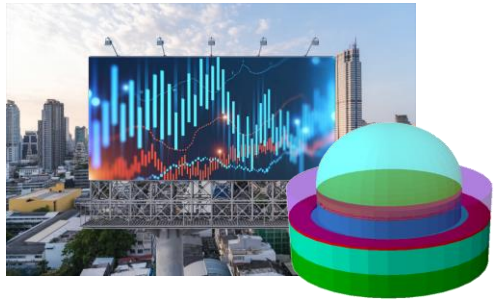
Strong user community in Israel, business support with Micon Global

Nov 2025: "Silvaco Group, Inc. (SVCO) is drawing significant attention in the technology sector, particularly from individual investors eager to capitalize on its potential upside of 57%".

Strong Industry Tailwinds Driving Adoption of Silvaco Platform

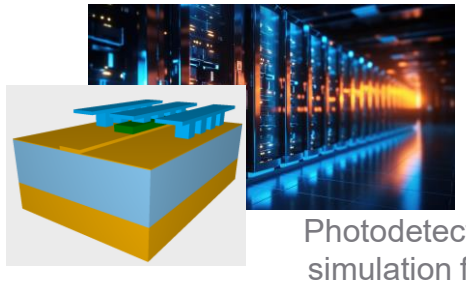
Emerging technology applications

- **Use and re-use of SIP to accelerate SoC TTM**
  - AI, HPC, Automotive, Industrial, and IoT
- **Industry adoption of new semiconductor materials**
  - SiC and GaN new materials for power devices
  - ReRAM and MRAM, new memory materials
  - Advanced CMOS designs for better SoC and SIP PPA
- **New Display technologies**
  - Mobile, wearables, automotive, gaming, virtual reality
- **Photonics adoption of new materials & technologies**
  - Waveguides, photo detectors, quantum dots, CIS

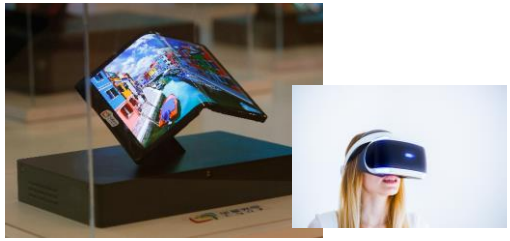


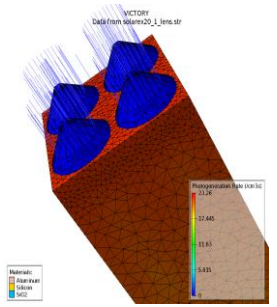
Micro LED and Quantum Dot Simulation

SiC, GaN Simulation for EV and Power Chargers

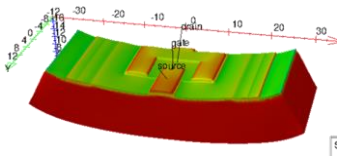


Photodetector simulation for integrated photonics





Solar Cell Simulation



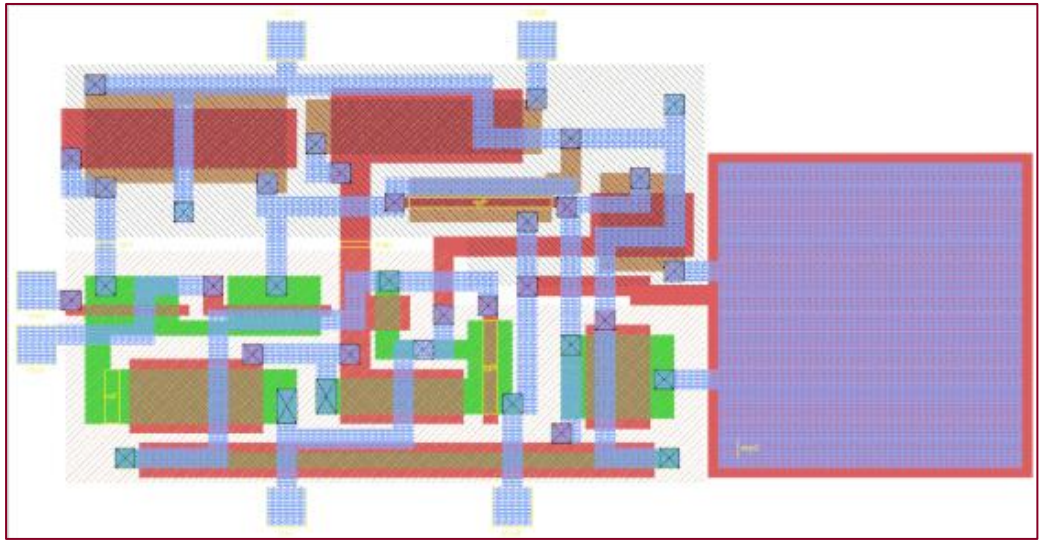
Flexible Display Transistor Simulation

Industry Need : Why Migrate Libraries?

- Where possible, developers will use foundry-provided, foundry-sponsored libraries
- But sometimes, something different is needed
- Maintaining a cell library, and migrating to a new technology node is a time consuming and error-prone

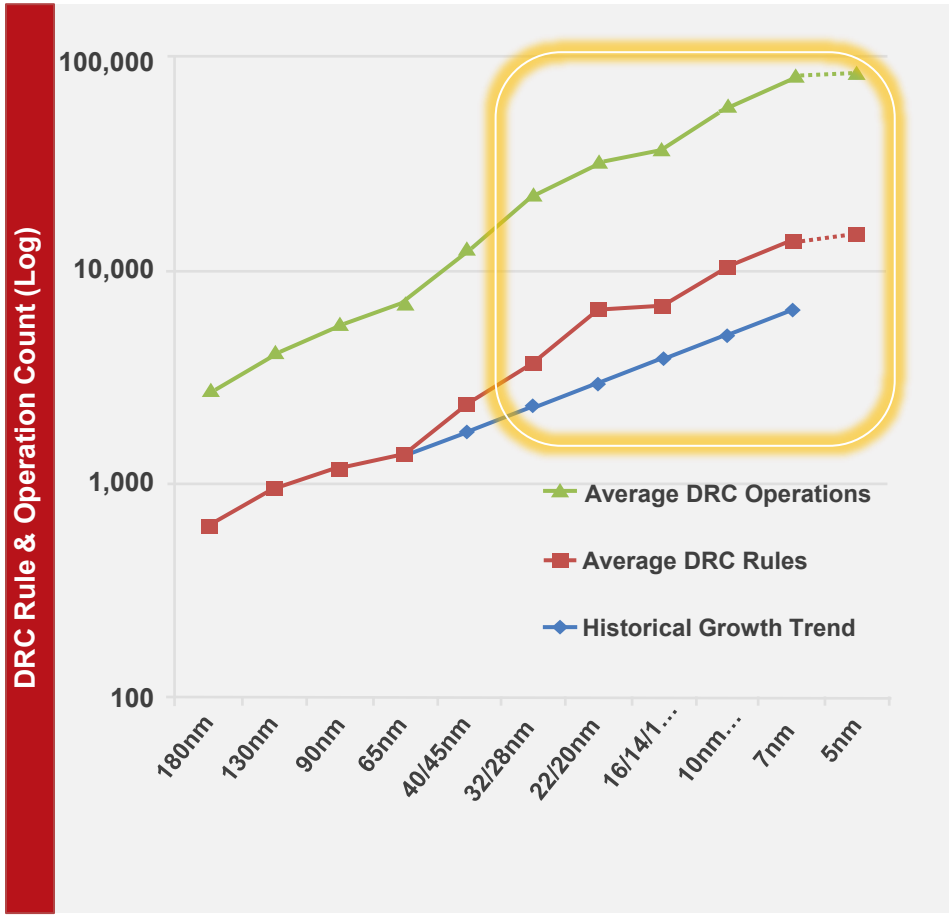
Customized Libraries :

- Non-Standard Voltage
- Ultra-Low Leakage
- Ultra-Low Power
- Optimized for Power, Performance, Area

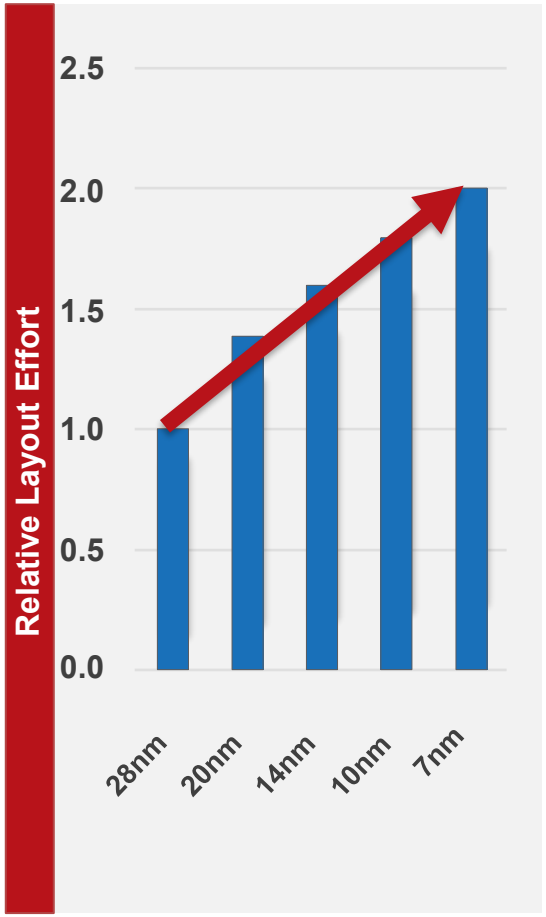


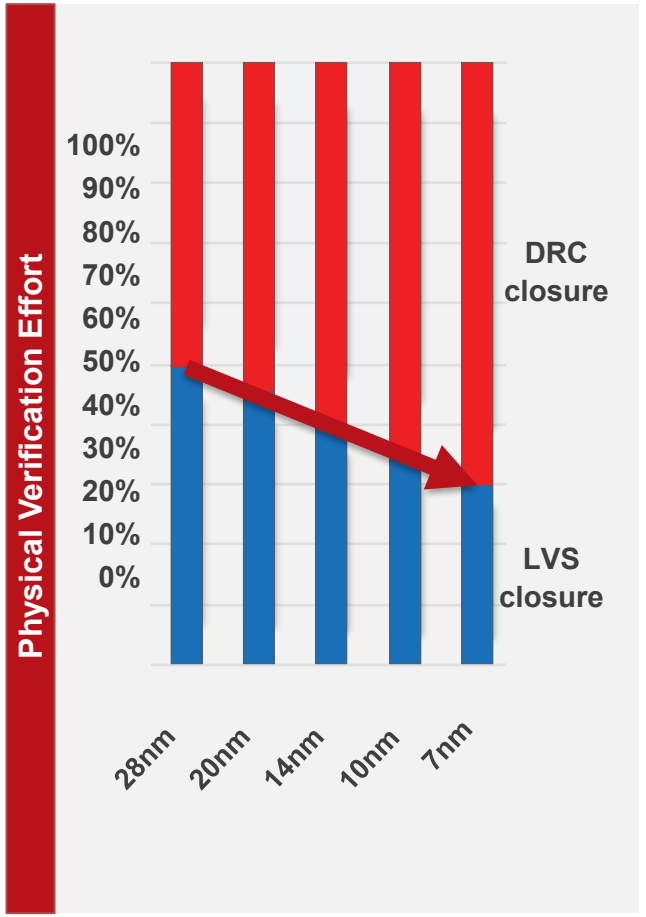
DRC Closure Increasingly Challenges Layout Design Productivity

Increasing DRC Rules and Rule Interaction



"Design Rule Complexity Rising", in Semiconductor Engineering





M. Leary, "IP design in a 5G world," in *MIDAS Ireland Annual Conf.*, Nov. 2018.

Decreasing Design Flexibility and Increasing DRC Complexity

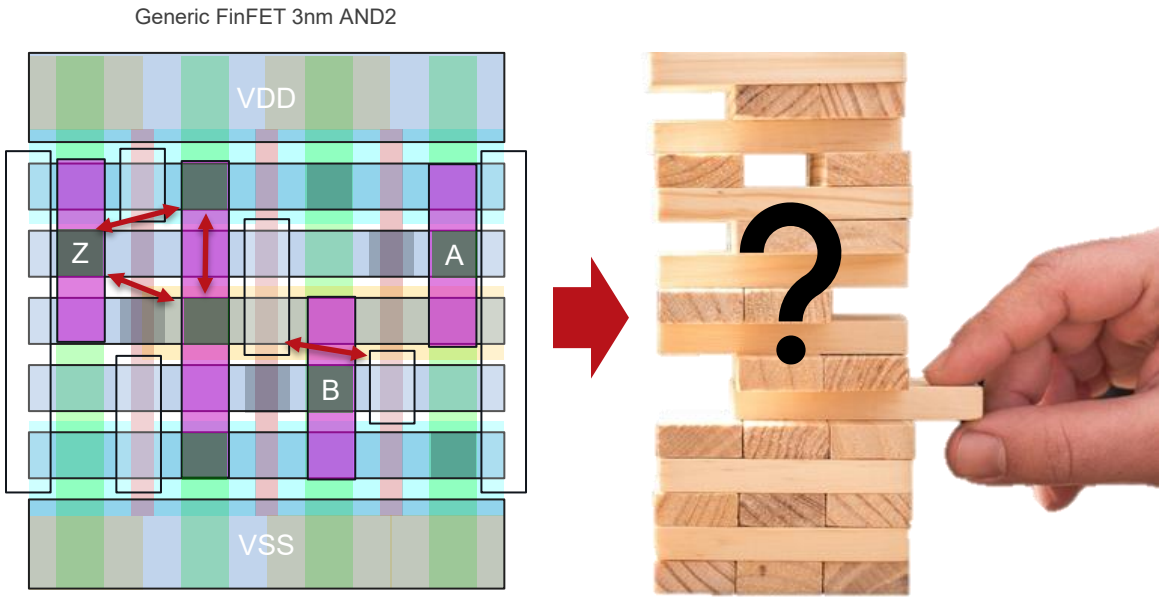
Challenges and Opportunities in FinFET Layouts

Increased design rule complexity

- Multi-patterning design
- Complex interaction between rules
- More border constraints

Reduced design flexibility w/ FinFETs

- Width quantization (number of fins)
- Limited routing freedom
- Complex cut patterning



DRC violations are local, but local “fixes” often lead to cascading effects

Empowering Layout Engineers Through Automation

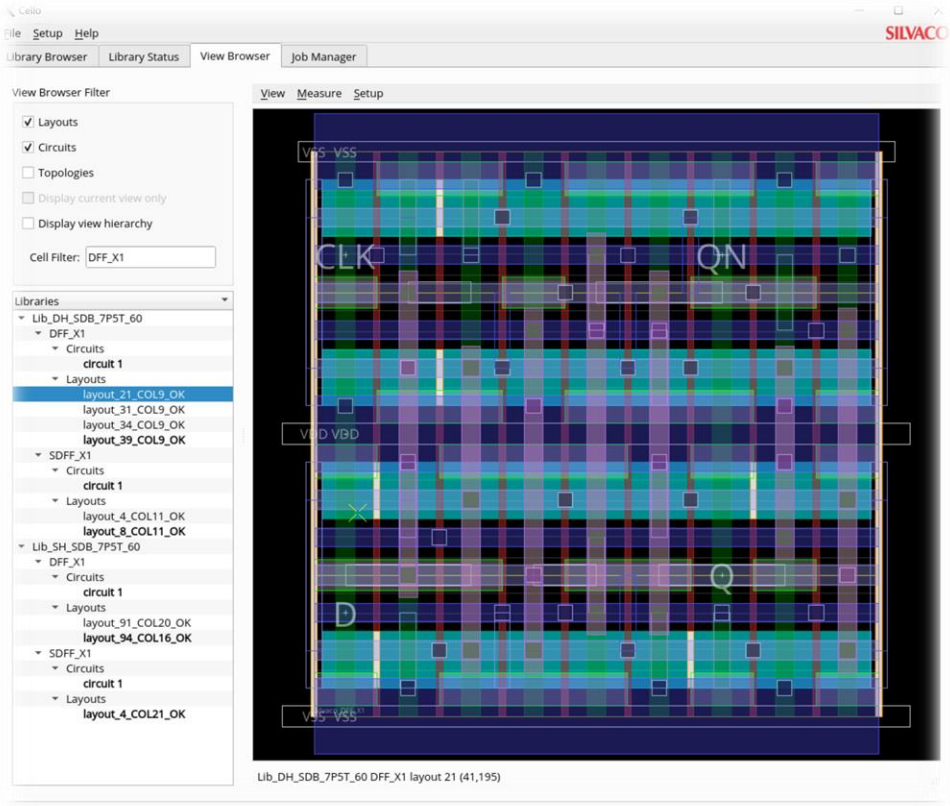
CellForge 3D Targets Advanced, sub-10nm nodes

Automated CDL/GDS to GDS generation

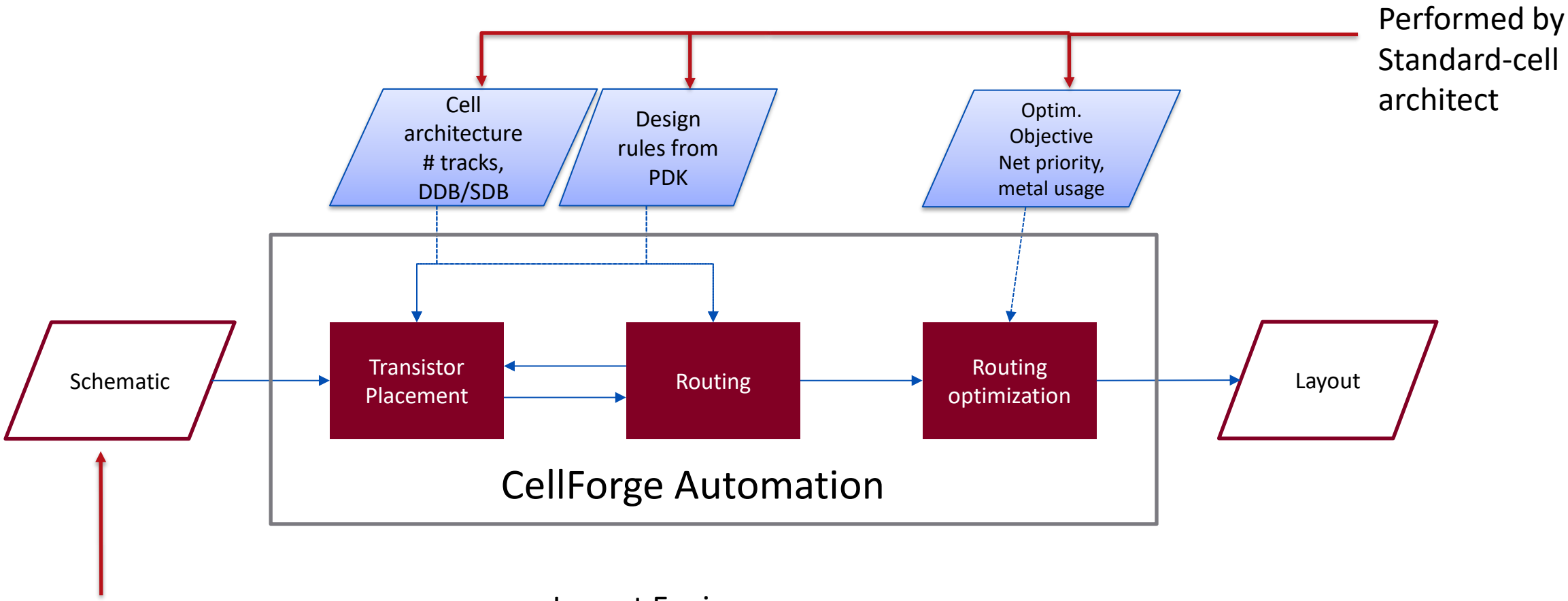
TCL API for Customization

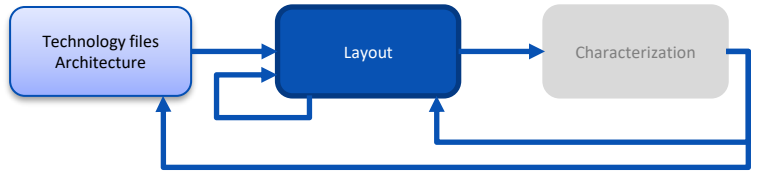
CDL and GDSII management

Integration with Verification tools



Automating with CellForge – How it works



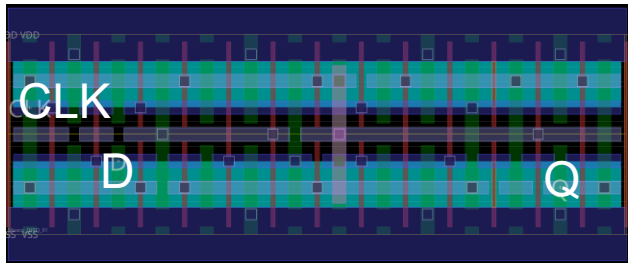


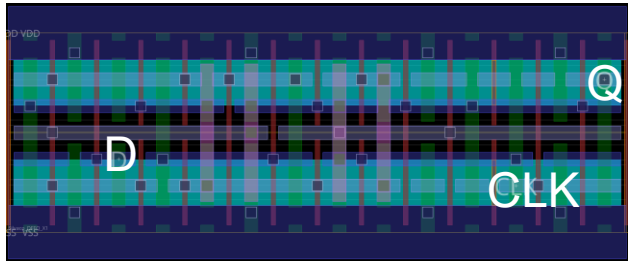
Automate Place & Route to Accelerate Cell PPA Evaluation

Generate multiple solutions with user-defined optimizations

Find out the best solution for each chip design

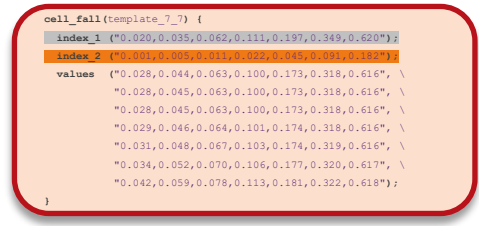
CellForge (Translate)

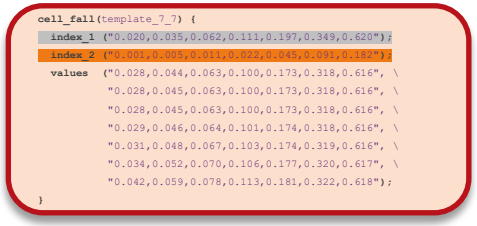




LibertyForge (Characterize)

- Timing
- Power
- Area

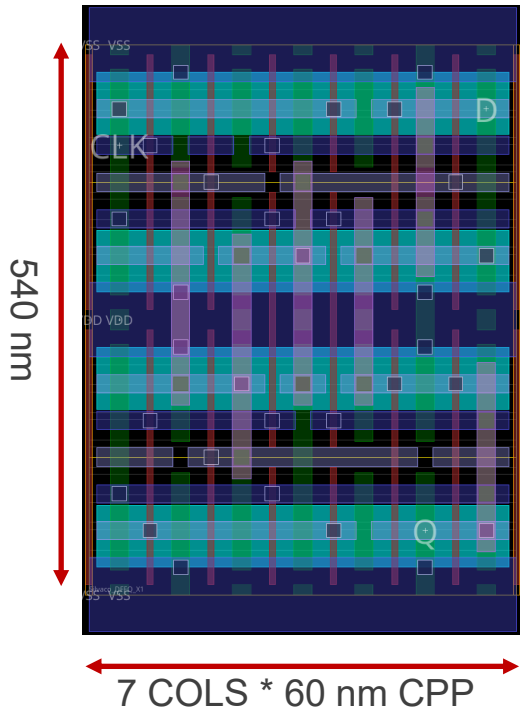




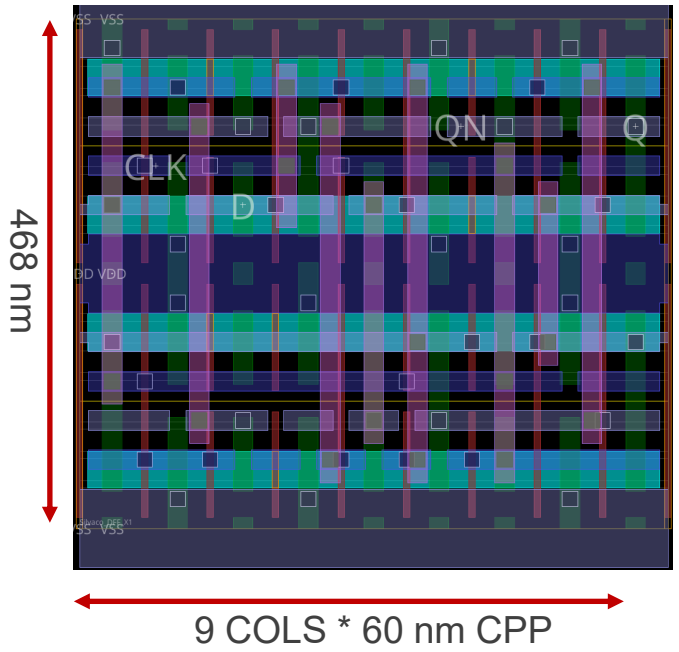
Enabling Fast and Effective Cell-Level DTCO Exploration

Compare different design architectures

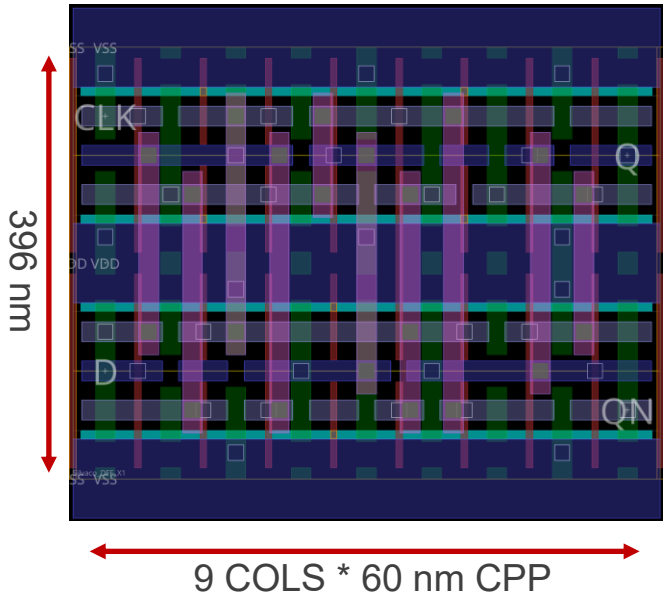
- 5M1 + 1T1 M2 gear



- 4M1 + 2T3 M2 gear



- 3M1 + 2T3 M2 gear

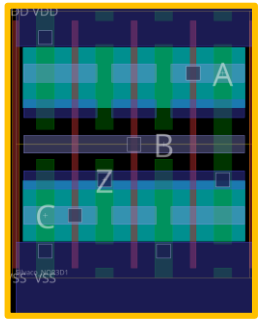


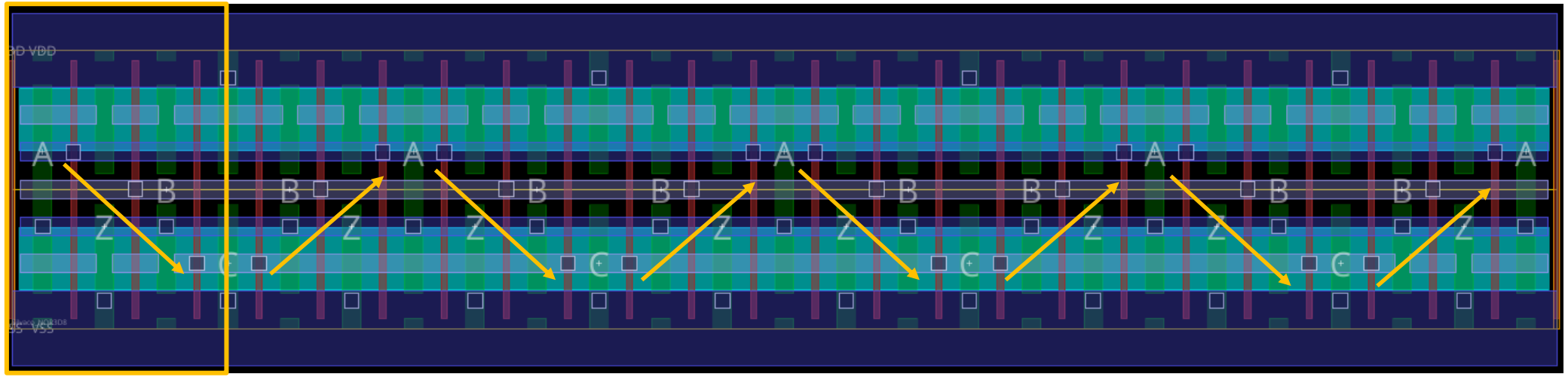
Augment Your Library Leveraging Existing Patterns

Reuse Placement and Routing for Faster Design Cycles

- Reduce creation time for larger cells
- Create consistent cell design across drive-strengths
- Reuse *seed* cell designs both routing and placement

seed





Success Stories

Optimizing PPA and Improving Productivity

3% better timing and without impacting area

- A leading semiconductor company's custom silicon team needed 3% better timing for their 3nm library
- CellForge 3D met this goal while maintaining or reducing cell layout area
- The company now plans to use CellForge 3D for their 2nm design

3X more productive over manual design

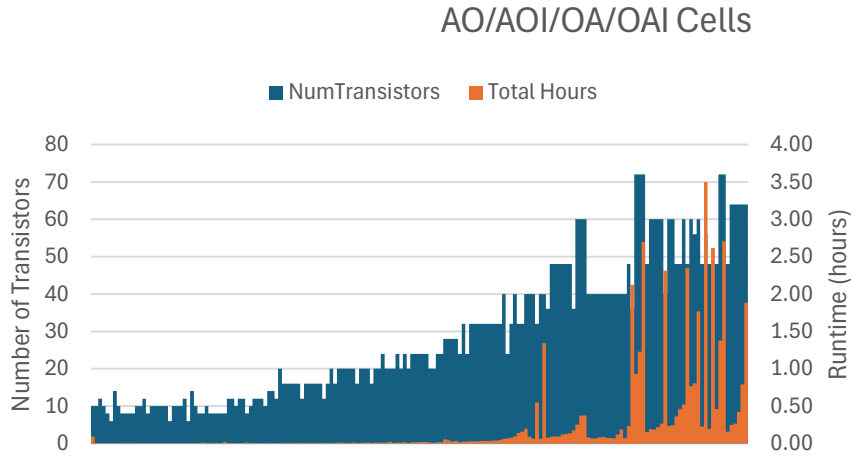
- Silvaco's IP development team designed a low-voltage library on 3nm
- Successfully built a library with breakthrough power efficiency and performance
- Team saw a 3x productivity improvement over manual design

Success Stories

Optimizing PPA and Improving Productivity

60k layouts generated in less than 6 months!

- Customer needed a faster datapath-sensitive library development flow
- CellForge 3D Accelerated Library Development Significantly:
  - Generated 60k GDS layouts in 6 months from a 1600 seed cell library
  - Majority of cells generated in less than 10 minutes
- Led to better PPA outcomes
  - Delay improvements up to 7%
  - 20% savings in M2 metal routing, significantly alleviating routing density
- Explored 20+ alternative architectures in 6 months



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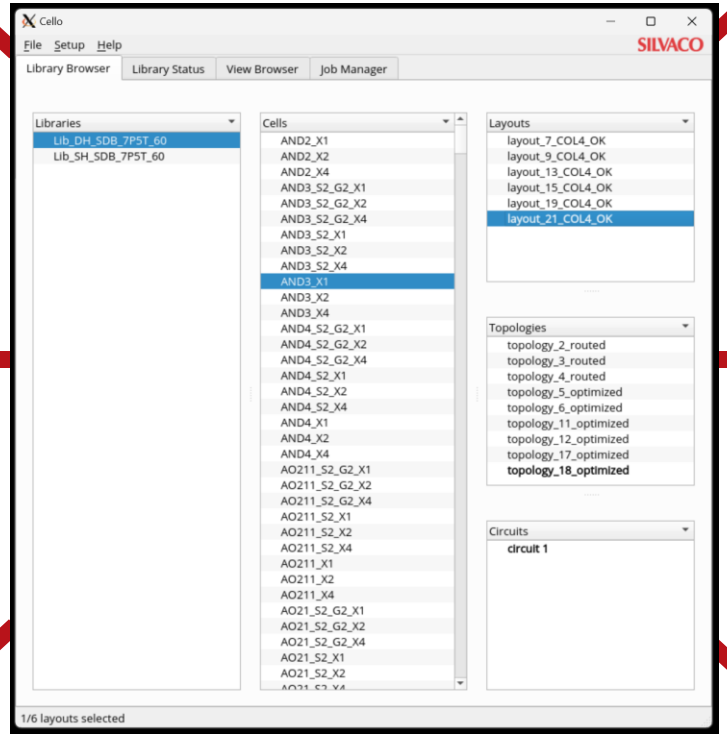
Summary of Automation Capabilities

AUTOMATED DESIGN FLOW
CDL to GDSII
GDSII to GDSII

CONFIGURABLE CELL DESIGN
Single and double diffusion break
Single and double height
Number of horizontal routing tracks
Number of metal levels

DTCO EXPLORATION
Backside power and signal routing
Layout impact of design rules
Emerging nodes exploration



PLACE & ROUTE CONSTRAINTS
Metal, via, and cut multi-patterning
Dummy and V_T spacing
Border constraints

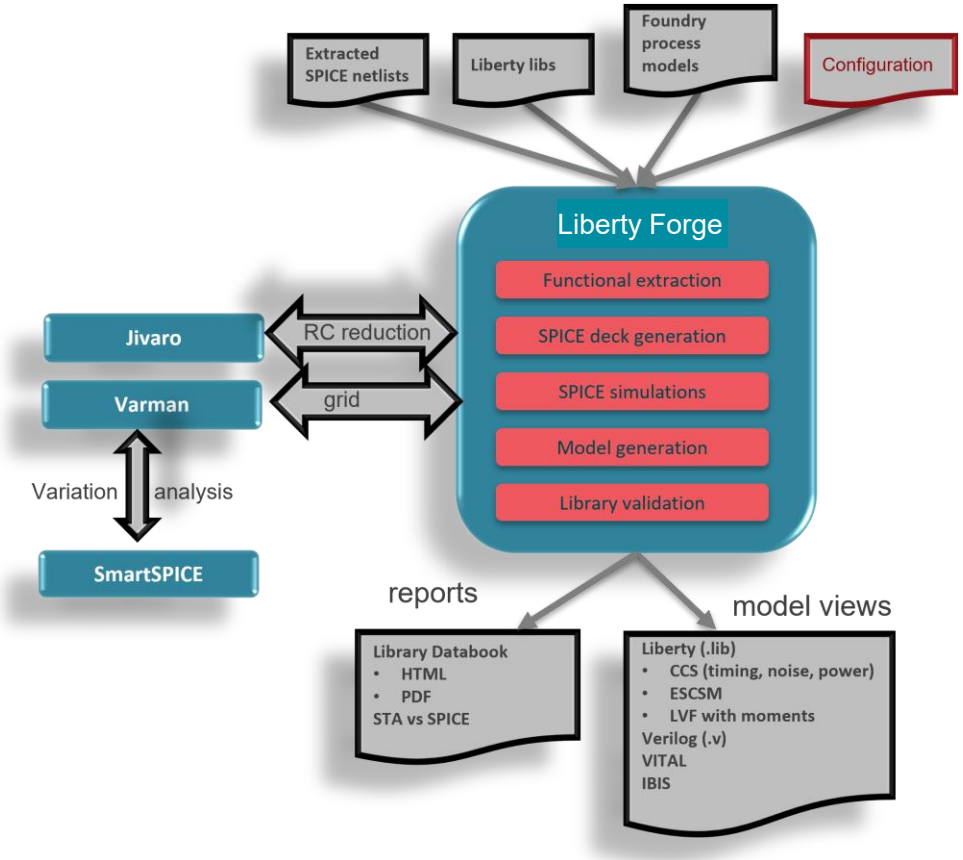
CUSTOM OPT. OBJECTIVES
Number of vias
Total routing wirelength
Number of columns
Custom layout-based criteria

FAST TURN-AROUND TIME
Automate library augmentation
Improve PnR results with specialized cells

Charcterization : LibertyForge

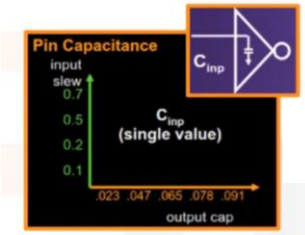
Ensuring Design Success through Accurate Cell Modeling

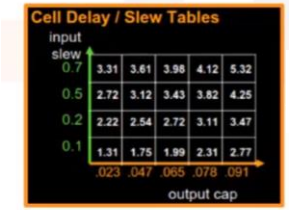
- **LibertyForge** is a bridge between semiconductor process technology and the rest of the EDA flow.
  - ➢ Standard cells = models timing, power, noise, and variation characteristics with high precision.
  - ➢ Memories = models timing and power for instances and memory compilers



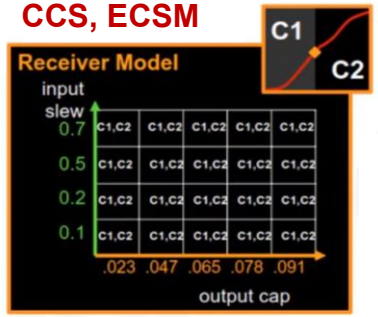
Liberty (.lib) timing and power models

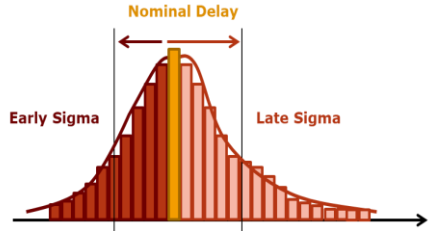
NLDM, NLPM





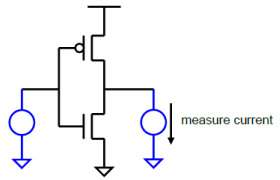
CCS, ECSM



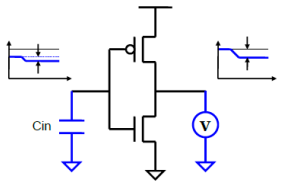


Process variation with moments (LVF)

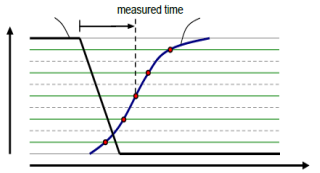
Composite Current Source Noise (CCSN) models



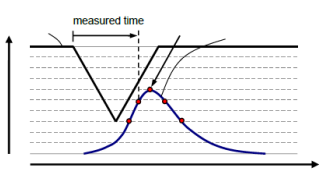
DC current tables on input and output stages



Miller capacitance



V(t) on input and output stages



Propagated noise

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Thank you

Contact : andrew.patterson@silvaco.com

Visit us at Booth #25

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Abstract:

As foundries continue to develop processes and support for FinFet and GAAFet technologies, the global demand for complex SOCs continues to increase, addressing the market demands for ever more capable AI and HPC applications. Design houses are looking for ways to improve their end-product performance, and keep up with evolving design-rules.

In this presentation, Silvaco will present how existing cell libraries can be migrated to new nodes and architectures. These migrations can keep existing placements and routing, update routing only, or create completely new cell layouts from existing CDL files. Silvaco will also show how complementary IP may be included, to optimize the engagement with a given foundry.