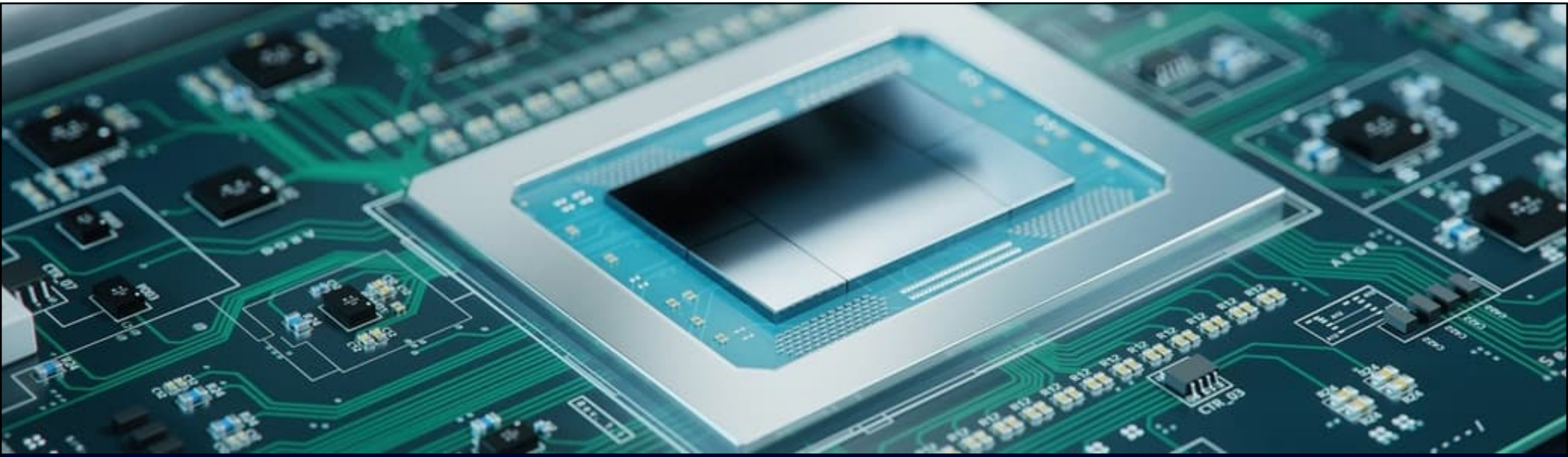

# Accelerating High-Performance SoC Development with Siemens EDA and Arm: A Software-Aware Verification IP Approach

Ofer Shagray, Verification Expert, Siemens EDA



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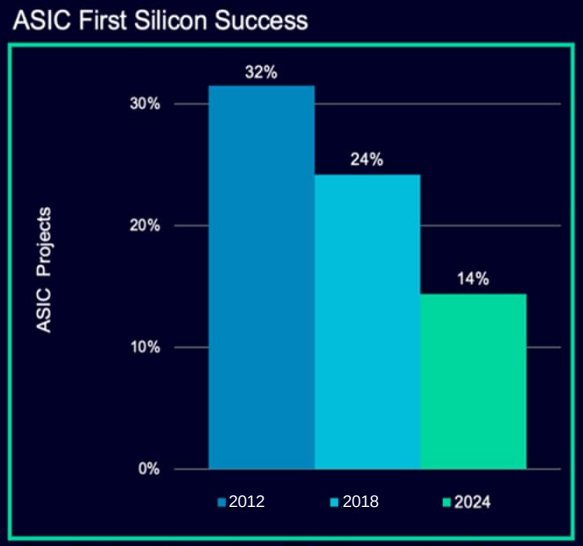
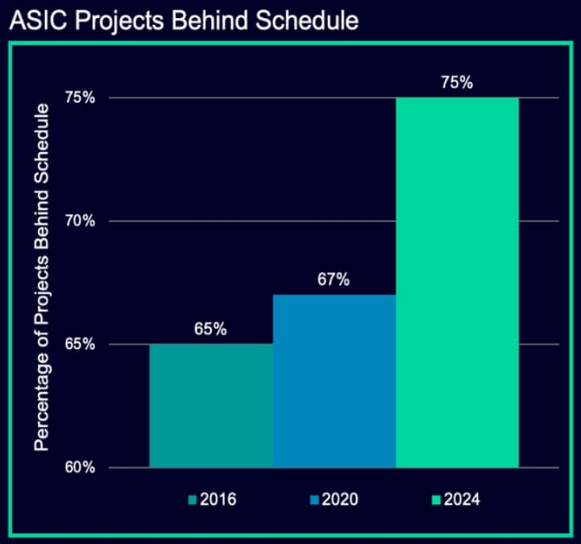
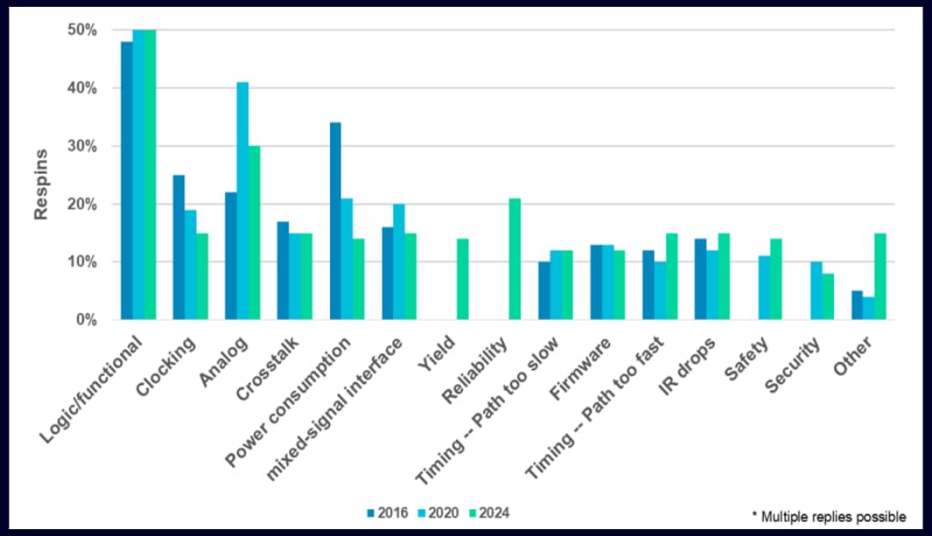
## Verification and Tapeout Challenges

ASIC projects increasingly suffer from first silicon BUGS, RESPINS, schedule SLIPPAGE




Source: 2024 Wilson Research Group IC/ASIC functional verification trends

Solving this problem necessitates a modern, collaborative, open standards approach:
Creating an intrinsic SHIFT LEFT, increasing confidence, reducing time

Siemens EDA Has Solutions

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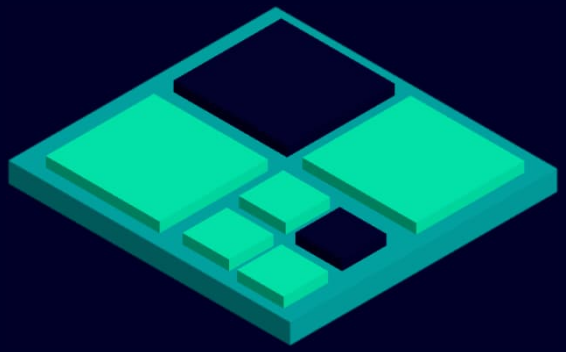
## Chiplets Revolutionizing System Design
Necessitates a modern Shift Left approach for AI System



Chiplet : New building blocks of computing

AI as the full stack requires aggressive “Shift Left” for competitive advantage

Pre-verified Compute Subsystem

Early SW Optimization

Co- validation of SW/HW

Siemens EDA Has Solutions



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# Siemens EDA Solution : Accelerating Arm Neoverse V3 CSS SoC Development

## Arm and Siemens EDA Collaboration
Arm Total Design (ATD) ecosystem

### Shift-Left Verification
- Arm Fast Models, QEMU
- Siemens Avery Verification IP
  (PCIe 7.0, CXL3.1, DDR5, HBM3E, UCIe3.0…)
- Siemens Software Aware VIP enabling
  SystemC/SystemVerilog co-simulation

### Multiple Applications
- BSA/SBSA compliance, ATP engine profiling
- PCISIG / CXLCV compliance
- Software / Firmware bringup
- Custom applications

### Scalable Design
- Multi-chip (C2C), chiplet (D2D) via PCIe/UCIe

### Benefits
- Fast bring up of CSS
- Early debug across HW/FW/SW
- Reduced risk and faster time-to-market

### Smooth transition from simulation to emulation
- Veloce high-speed hardware-assisted platform
- Avery VIP + VTL on Veloce = 50x acceleration
- Veloce System-level solutions – VLAB

# Shift-Left: Software Aware VIP (SAV)

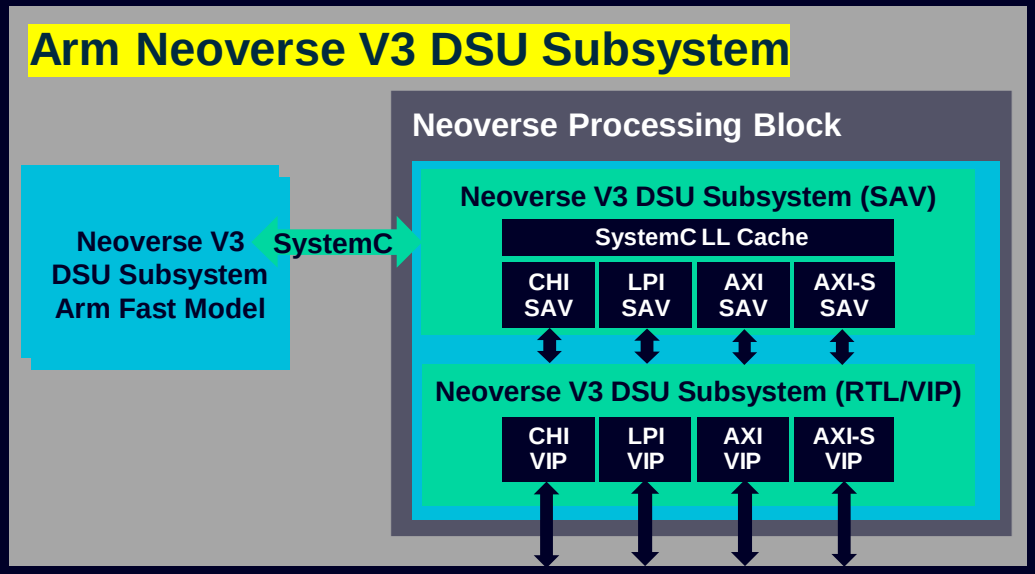
A simulation Testbench + VIP approach to HW/SW co-development

**SystemC Integration to ARMFM**

SystemC TLM2.0
Simulation Synchronization
SystemC Last Level Cache

**ARM Fast Model**

SBSA / BSA testing
Debug Trace Support
Cycle Approximate Processor




**Siemens Avery Verification IP**

Open Standards AMBA CHI
Class Based SystemVerilog
Dynamic Configuration
Randomization
Debug / Trackers
Protocol Checks
Interoperability, robustness
100+ customers / tapeouts
IP partnerships



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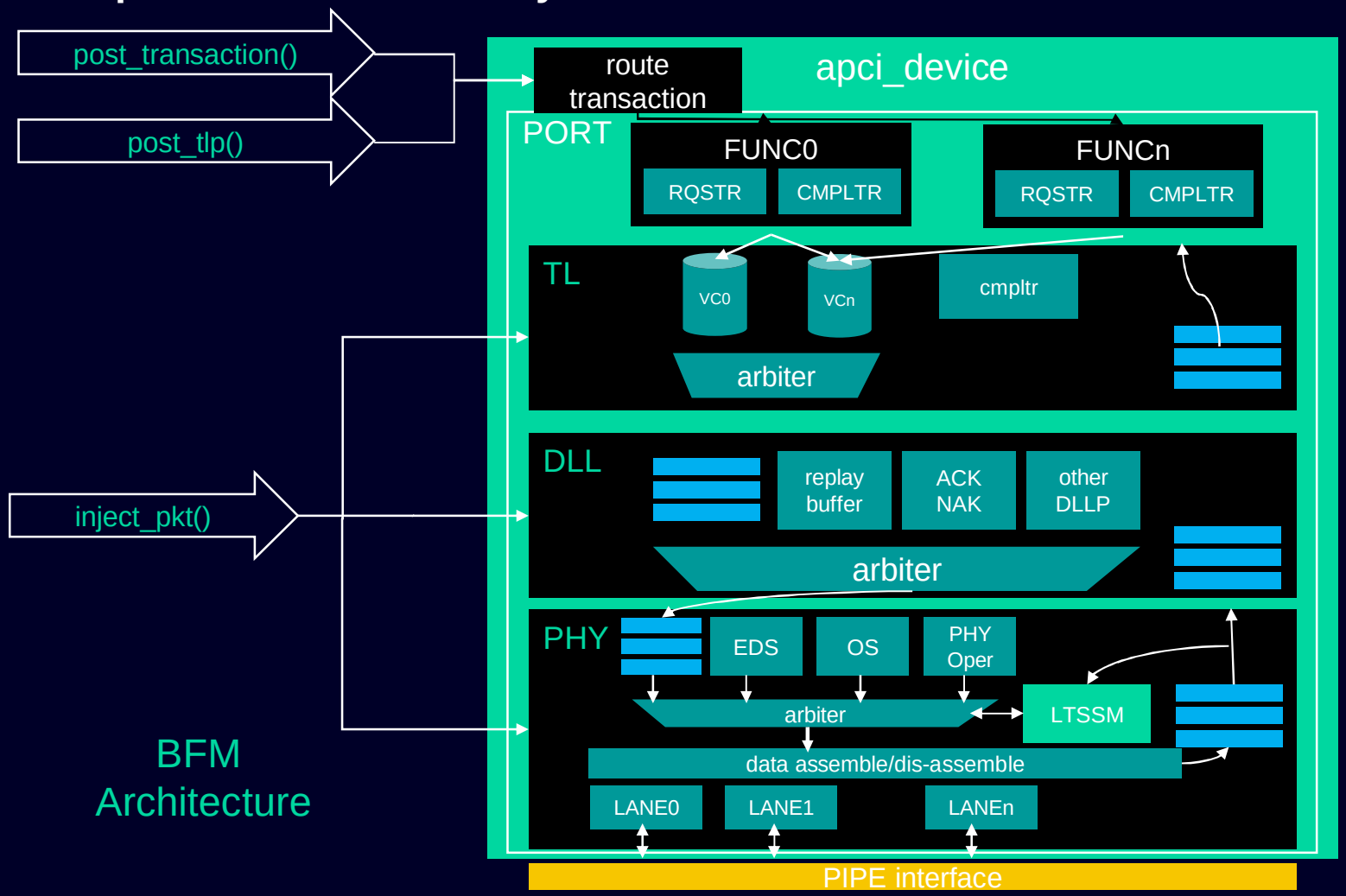
# Component: Siemens Avery Verification IP




BFM Architecture

## PCIe 7.0 Verification IP

- Class-based SystemVerilog
- Dynamic Configuration
- Randomization
- Advanced Error Injection
- Trackers | Debug
- Protocol Checks
- Veloce Acceleration Support



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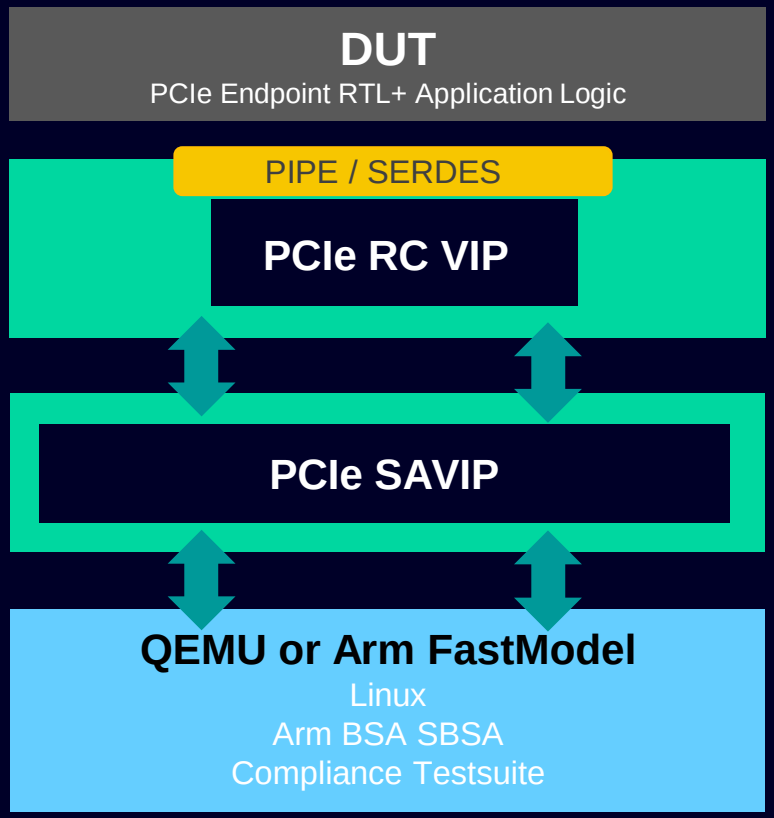
## Component: Siemens Software-Aware VIP (SAV)

Co-simulate RTL testbench and VIP with SW on Arm FastModels or QEMU models




**PCIe 7.0 Verification IP**
- Class Based SystemVerilog
- Dynamic Configuration
- Randomization
- Trackers | Debug | Protocol Checks

**SAVIP**
- SystemC TLM2.0
- Simulation Synchronization (DPI)

**QEMU or AFM model**
- Emulates Aarch64
- UEFI and OS boot
- BSA/SBSA compliance testing
- PCISIG / CXLCV



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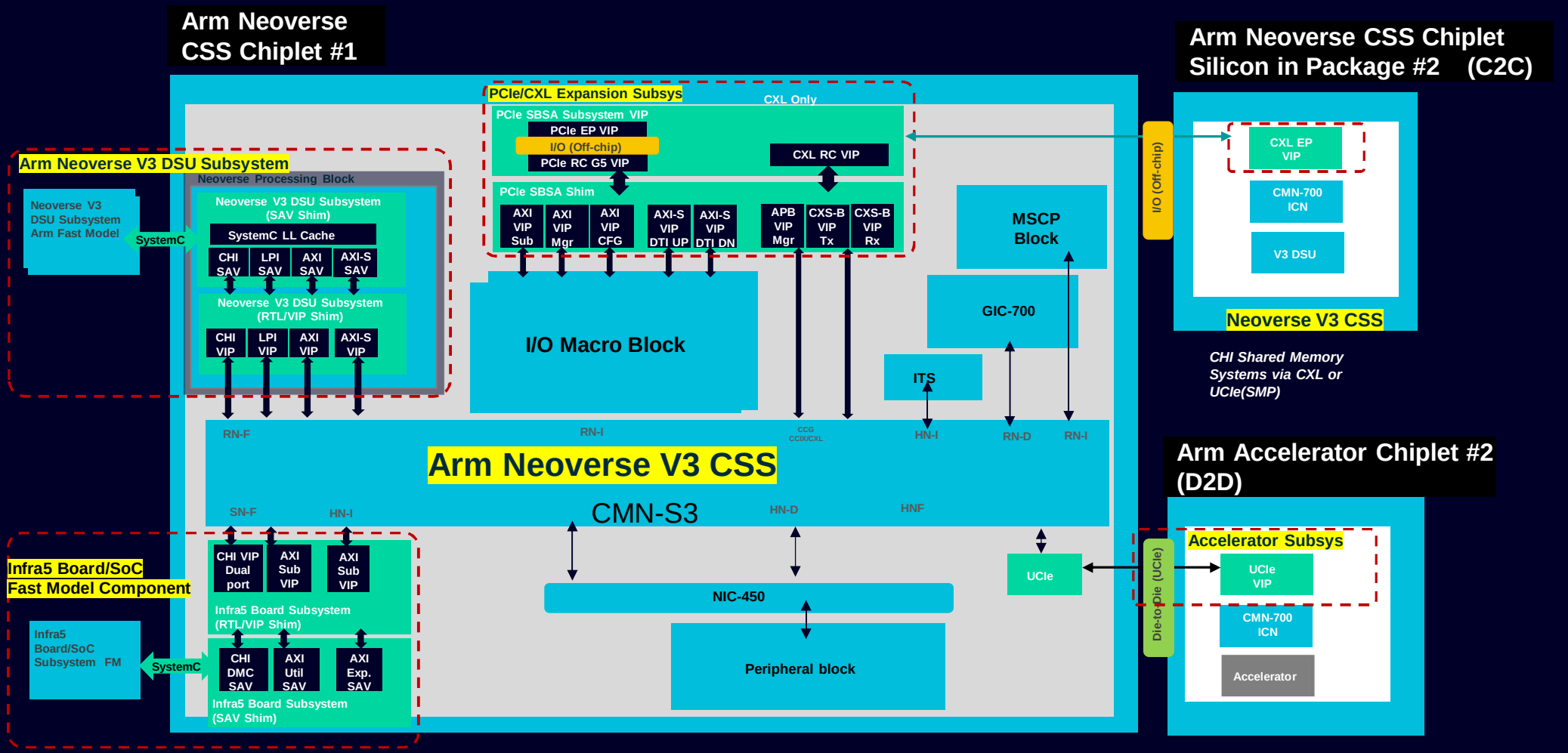
# **Putting it All Together** - Arm Neoverse CSS System + SW/FW Bringup



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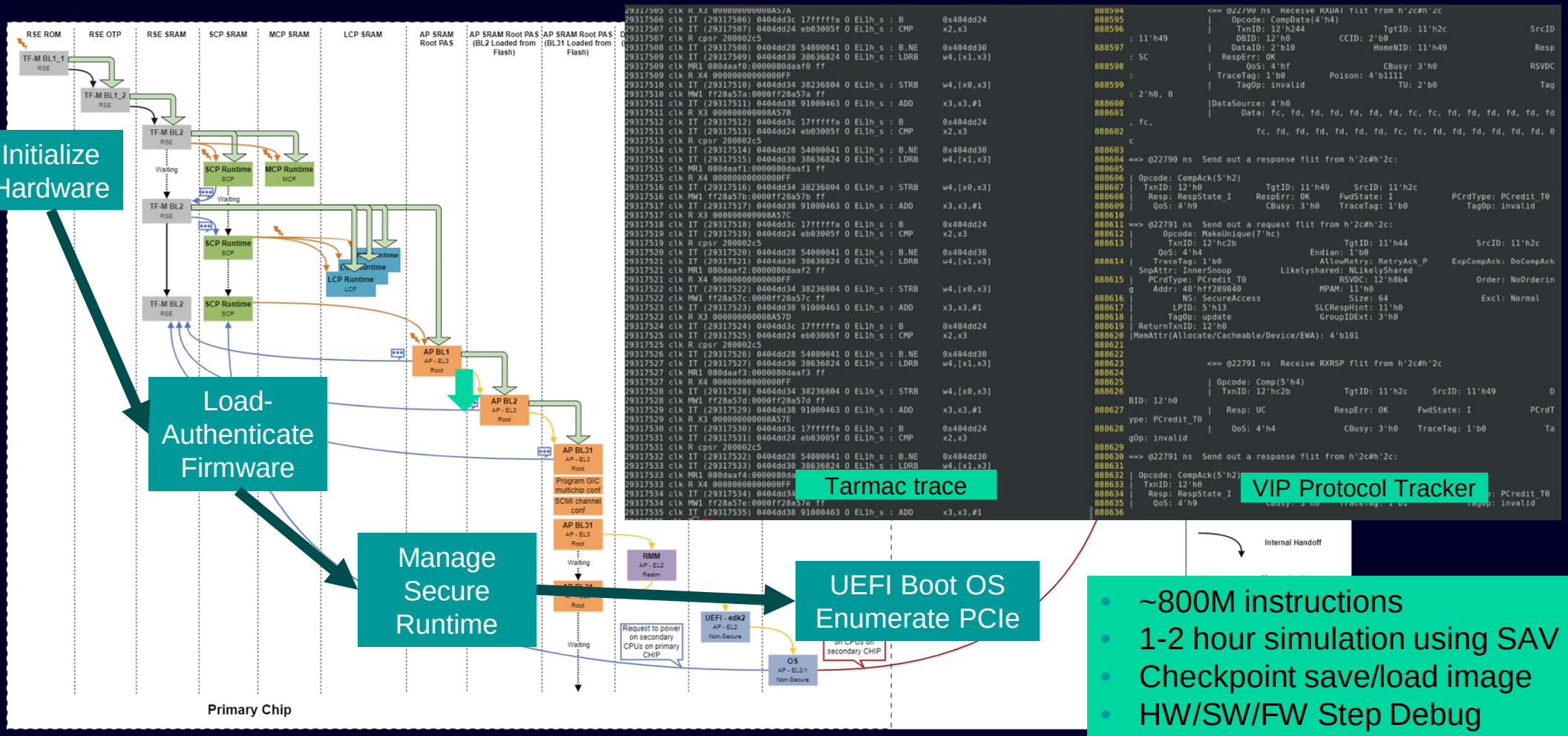
# Simulating ARM Neoverse N2 CSS Bootup, SBSA Testing




- ~800M instructions
- 1-2 hour simulation using SAV
- Checkpoint save/load image
- HW/SW/FW Step Debug

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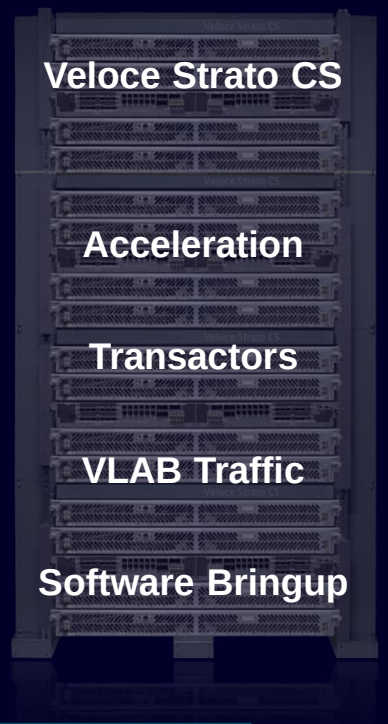
## Arm and Siemens ATD partnership for Neoverse CSS
Simulation-Emulation Continuum

- **RTL Simulation**
- **UVM Traffic**
- **Avery Protocol Verification IP**
- **Software Aware VIP (SAV)**

Smooth transition from simulation to emulation

Solutions that scale up as your project evolves




Arm and Siemens enable the joint ecosystem to accelerate verification and software bring-up for CSS-based system design



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## Disclaimer



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# Thank You

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