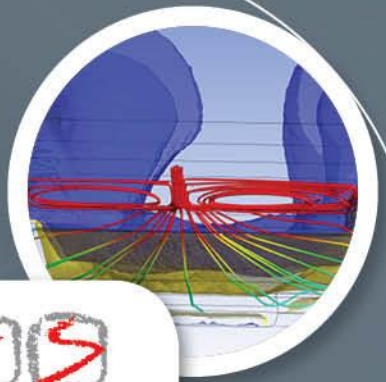

Computerized Analysis & Simulation Ltd

Cooling Challenges from Chip to Data Center Level

CAS Ltd. - Computerized Analysis & Simulation

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Semisrael2025

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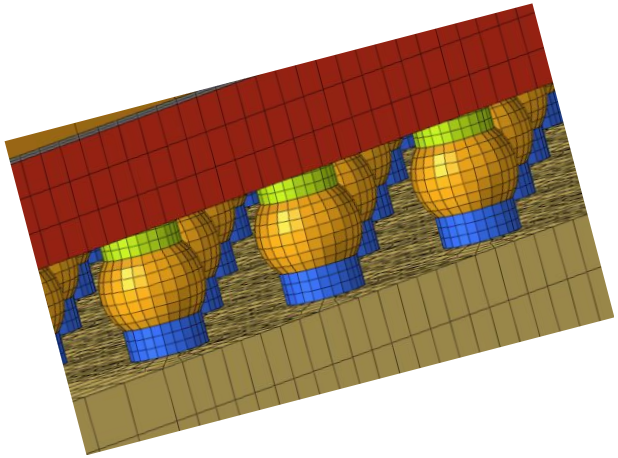
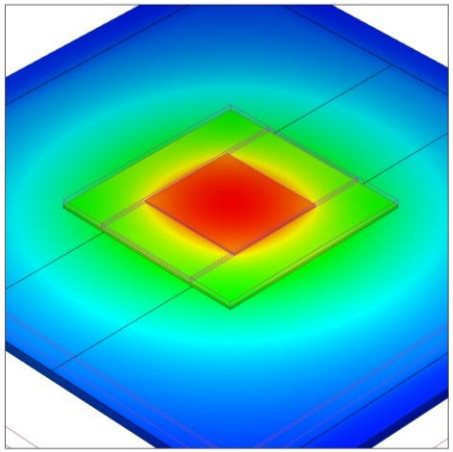
Who We Are

- *Innovative CA service provider in the field of mechanical, thermal, dynamical and CFD systems.*
- *Established in 1995, Today we are 12 workers.*
- *Specialization in providing a complete range of engineering consulting, starting from the first conceptual design, and up to the final testing stages, using cutting edge computerized tools such as, FE (Finite Elements) and CFD (Computerized Fluid Dynamic) software.*
- *Engineering Consulting, Conceptual Design and Simulation:*
  - *Mechanical*
  - *Dynamical and rigid body*
  - *CFD design aspects*
  - *Optimization*
  - *Thermal*
  - *Full system modeling*
  - *Multi discipliner*
- *Environmental and Verification Testing*
- *Marketing & Supporting – Simulation and CAD Software*

Introduction

- As computing power continues to grow—driven primarily by the increasing demands of artificial intelligence—cooling has become a critical challenge at every level of electronic systems, from individual chips to entire data centres
- At the chip level, rising power densities require advanced thermal management techniques, precise thermal design at the board and TIM levels, and optimized heat exchangers. At the server and rack levels, efficient heat removal depends on the coordinated design of airflow, liquid cooling loops, and component layout. At the data center scale, energy efficiency and sustainability rely on system-level strategies such as hot and cold aisle containment and advanced liquid cooling architectures





Way Thermal/CFD Simulations ?

By using system numerical model simulation (FVM/FEM) we can :

- **Early Identification of Thermal Issues** – Detect potential overheating or thermal bottlenecks before physical prototyping, reducing costly redesigns.
- **Optimized Thermal Management** – Enable engineers to refine the design,by Examining "what if" scenarios.
- **Reduced Development Time and Cost** – Minimize the number of physical prototypes and tests needed by validating designs virtually.
- **Improved Reliability and Performance** – Ensure components operate within safe temperature limits, extending product lifetime and stability and examining failure scenarios
- **Enhanced Design Insight** – Provide detailed visualization of temperature distribution and heat flow, supporting better design decisions.

Why Do We Need To Address The Temperature Difference Near To The Component?

- *Example:*

Electronic module with electronic component 14 x 10 mm , powered by 50 W

$$\Delta T_{TIM} = Q \; x \; R = \frac{Q \cdot \Delta x}{K \cdot A}$$

$Q = 50$ [W]

$A = 0.014 \text{ x } 0.01 = 0.00014 \text{ m}^2$

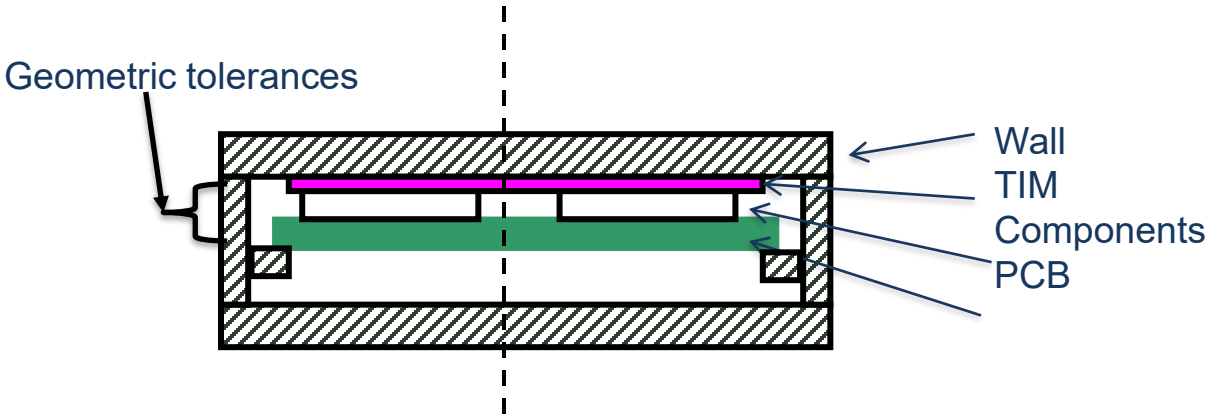
$K = 1$ [W/m · k]

$\Delta x = 0.001$ [m]

$$\Delta T_{TIM} = \frac{50 \cdot 0.001}{1 \cdot 0.00014} = 357 \; ^oC$$

$K = 10$ [W/m · k] $\Rightarrow \Delta T_{TIM} = 36 \; ^oC$

$\Delta x = 0.0005$ [m] $\Rightarrow \Delta T_{TIM} = 18 \; ^oC$

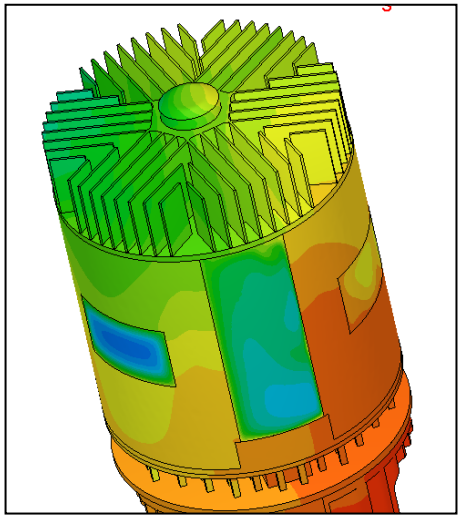


Electronic System Design Workflow

- *Requirement verification*
  - *Base line design- Important !*
    - *Power*
    - *Environmental conditions*
    - *General allowable temperatures*

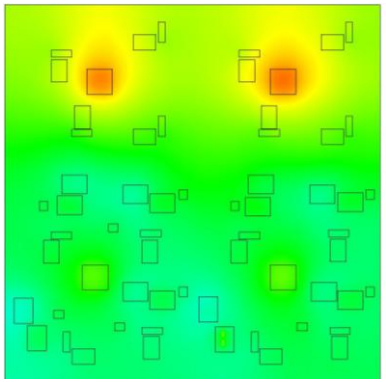
Desigen space

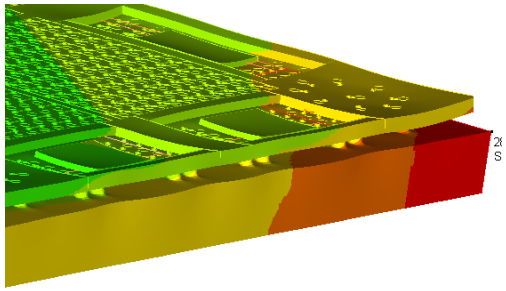
- *Concepts*
  - *No mechanical/electronic model yet*
- *Preliminary design ("PDR")*
  - *Basic design data*
- *Detailed design/verification ("CDR")*
  - *Final mechanic*
  - *Final placement layout and layer*

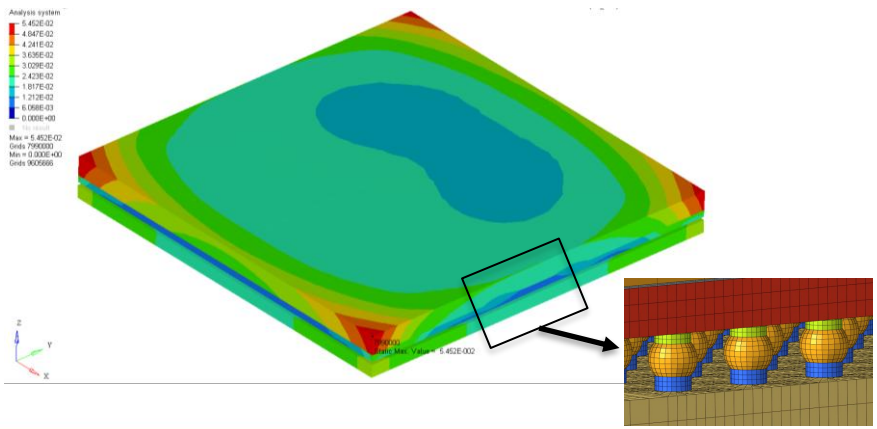


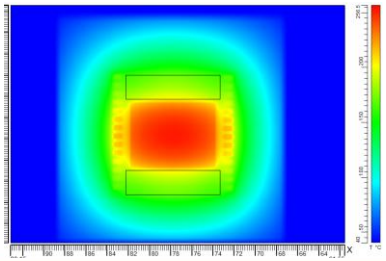
Chip Level Simulation

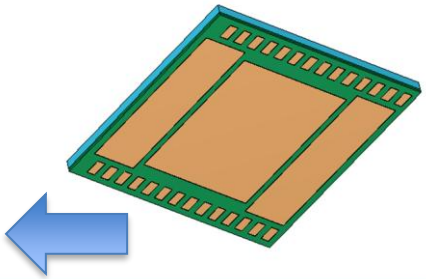
- Power densities
- Heat slag
- Via
- Thermal expansion
- Substrate conductivity
- PCB component cross talk
- θjc, θjb, θja Test



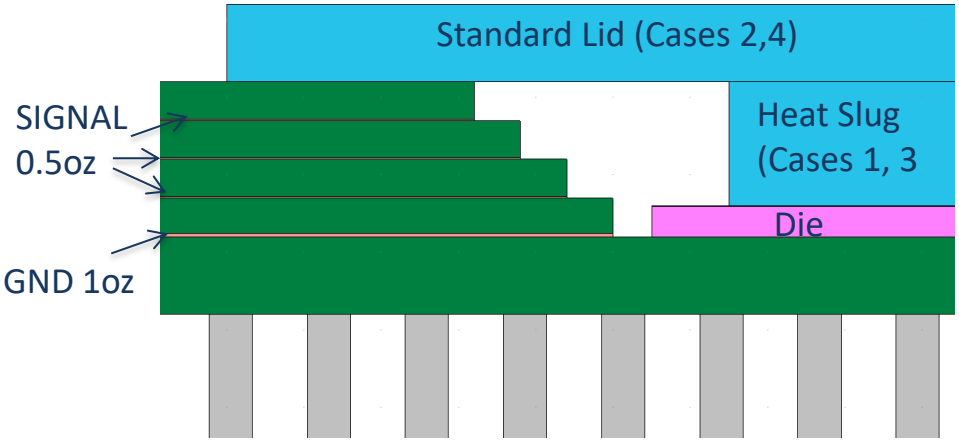


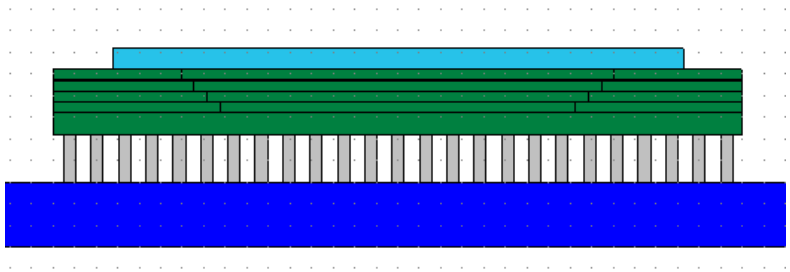


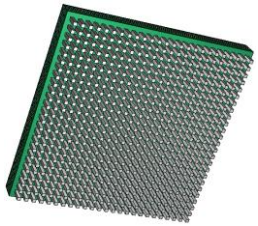


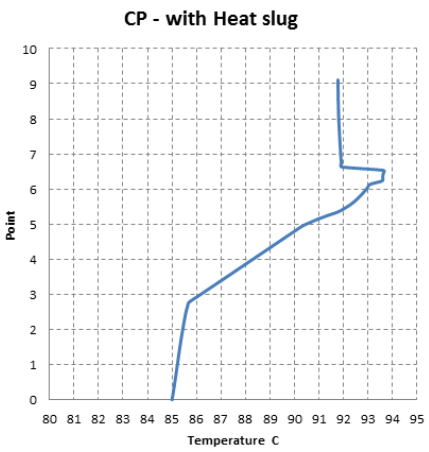


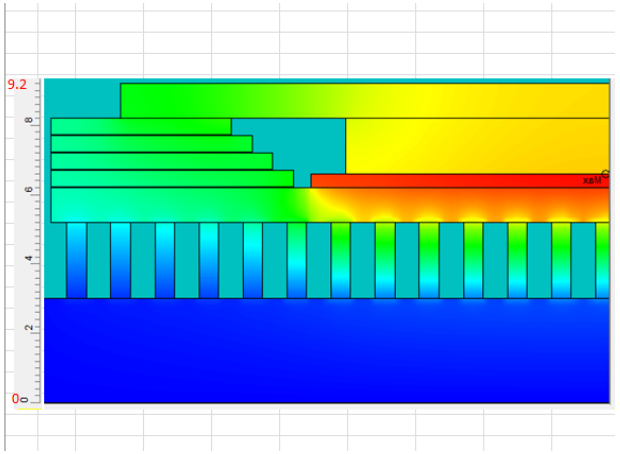
Chip/Packaged Level Simulation



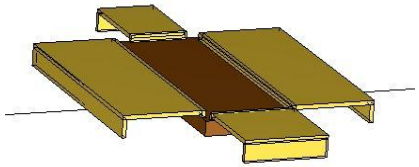


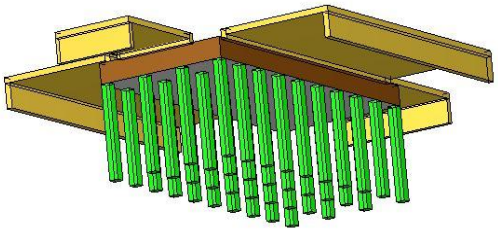


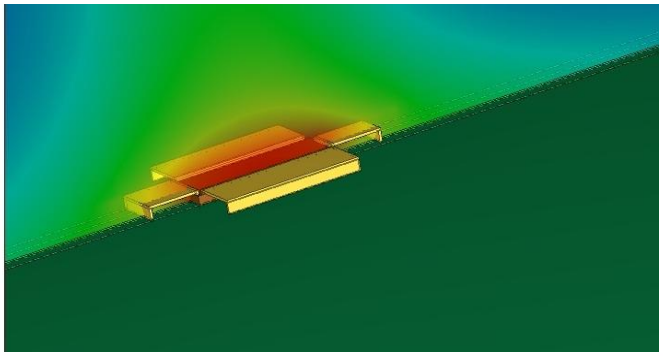


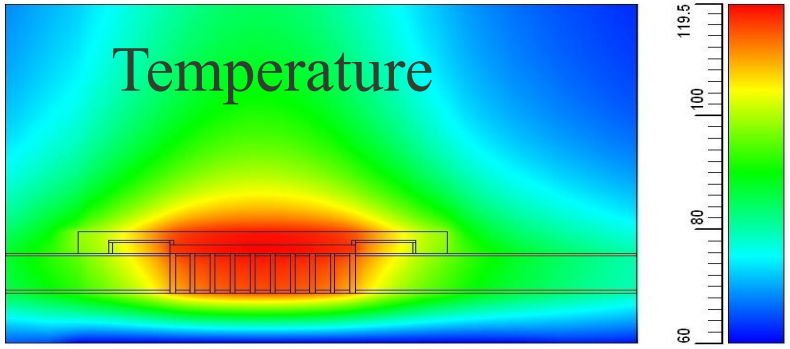


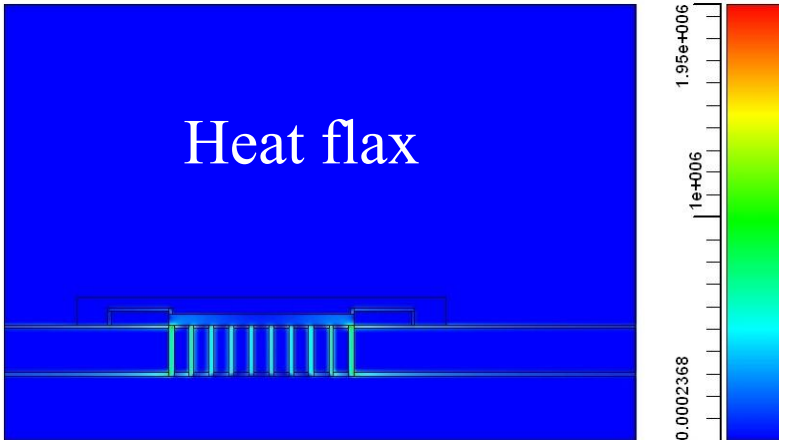
Chip/Packaged Level Simulation
Thermal Via Influences





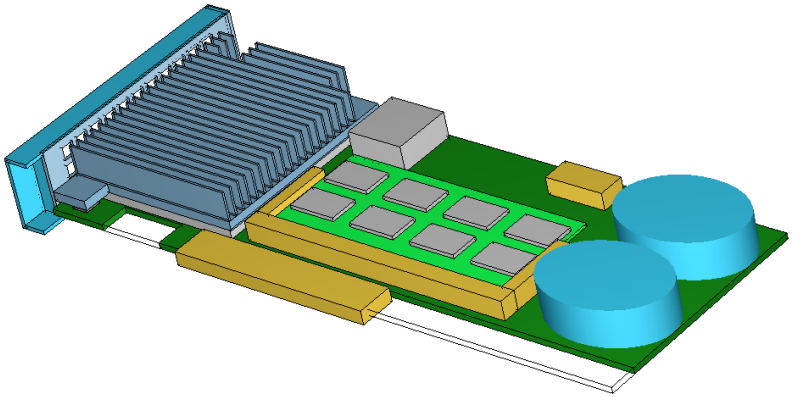


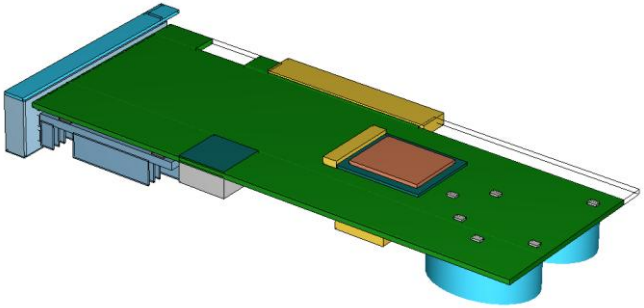


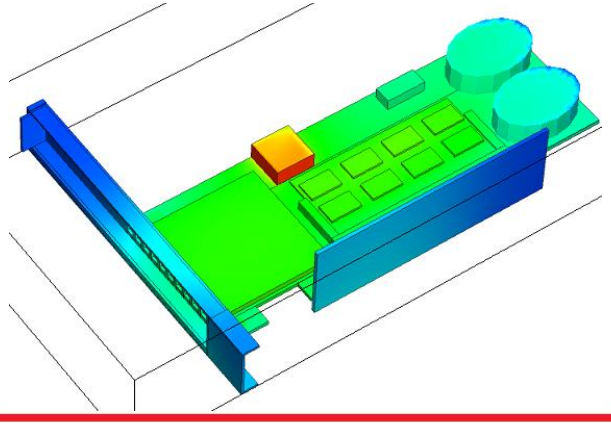


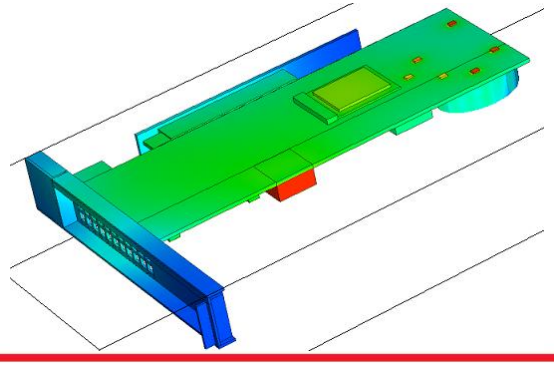
Card Level – Simple Example

PCI – HHHL – Model and temperature map at 250 LFM



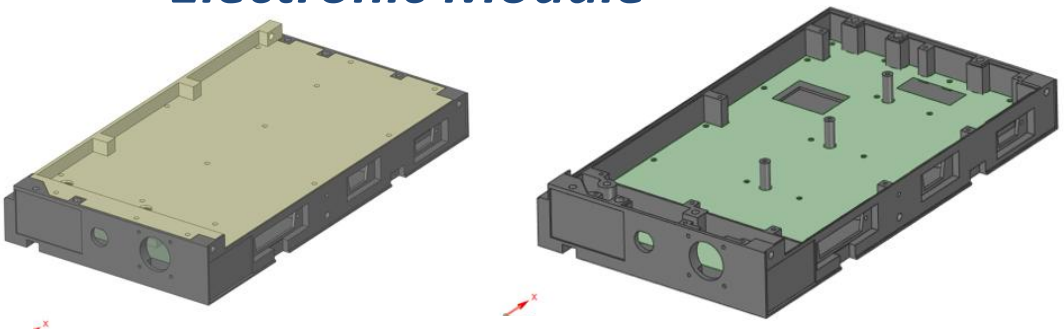


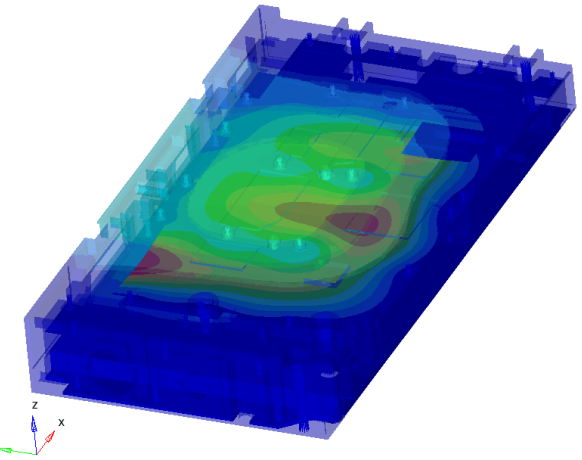




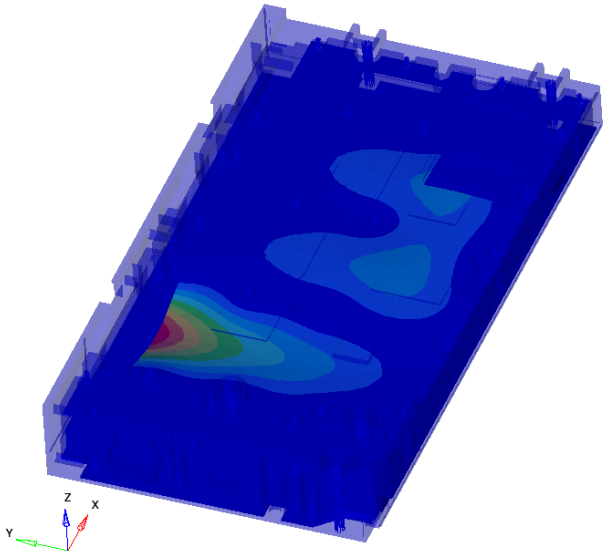
Card Level - Dynamic - Modal Analysis

Electronic Module

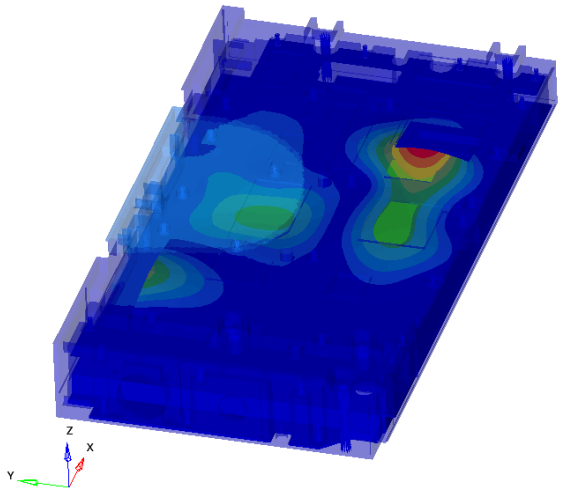




Mode 1 – 392 Hz



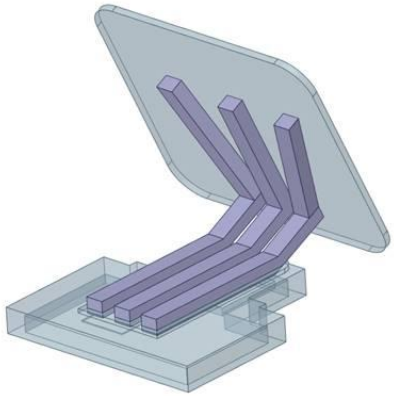
Mode 2 – 455 Hz

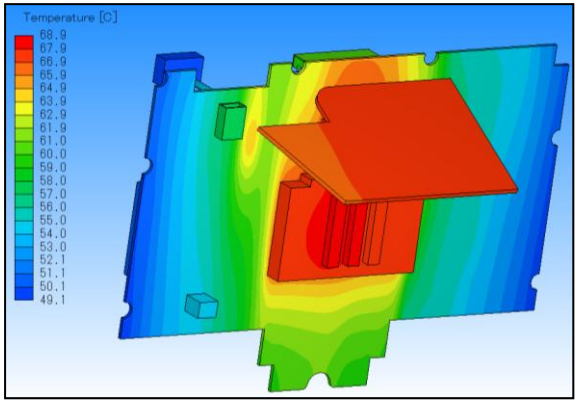


Mode 3 – 529 Hz

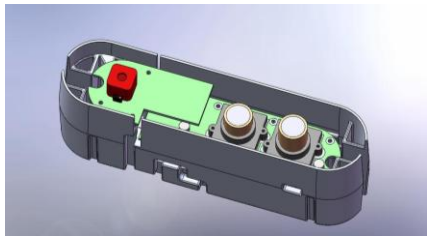
Advance Cooling Techniques

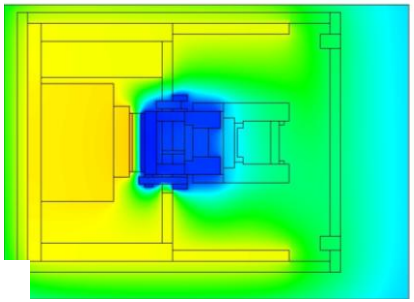
- **Heat pipe/Vapor chamber**
  - High conductivity due to boiling process



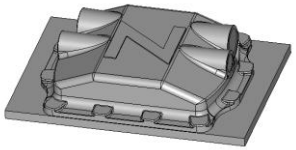


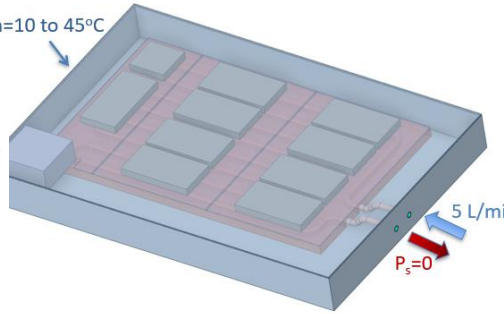
- **TEC** – active cooling
  Low efficiency

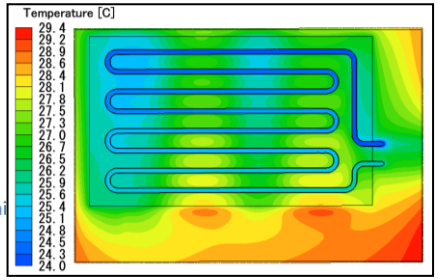




- **Liquid cooling**
  - Regular
  - Two-phase liquid cooling
- **Graphite/ Graphene**

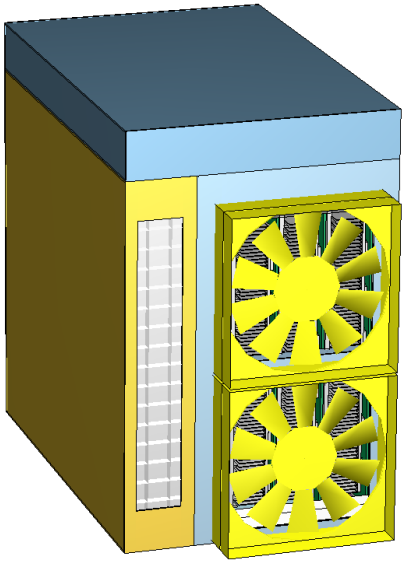


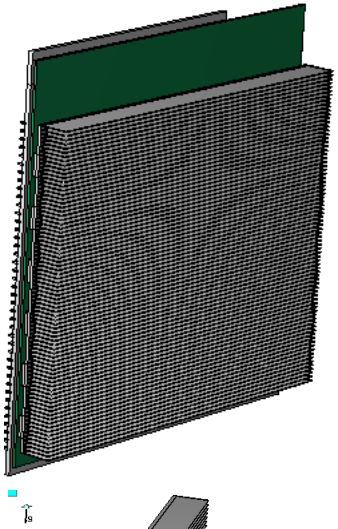


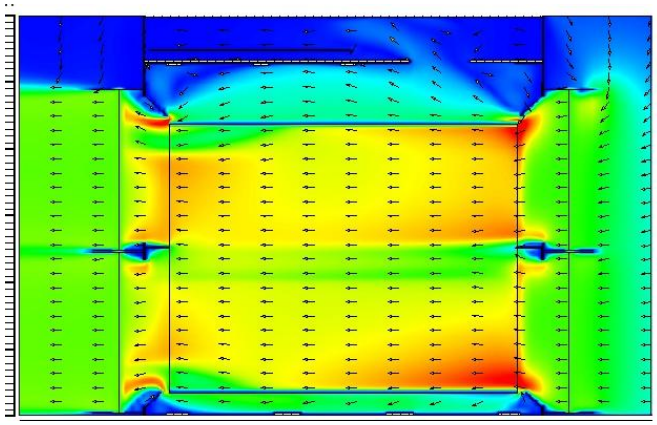


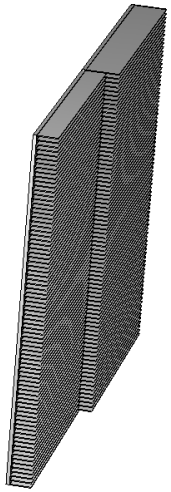
- Cooling powder ☺

Chassis Level – “What If Case “









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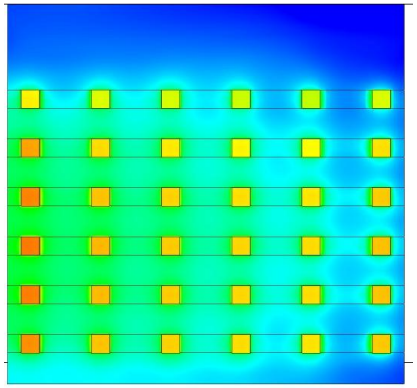
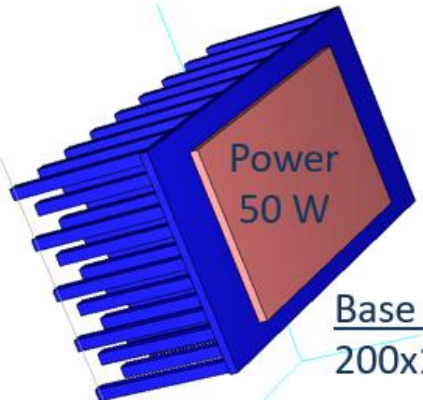


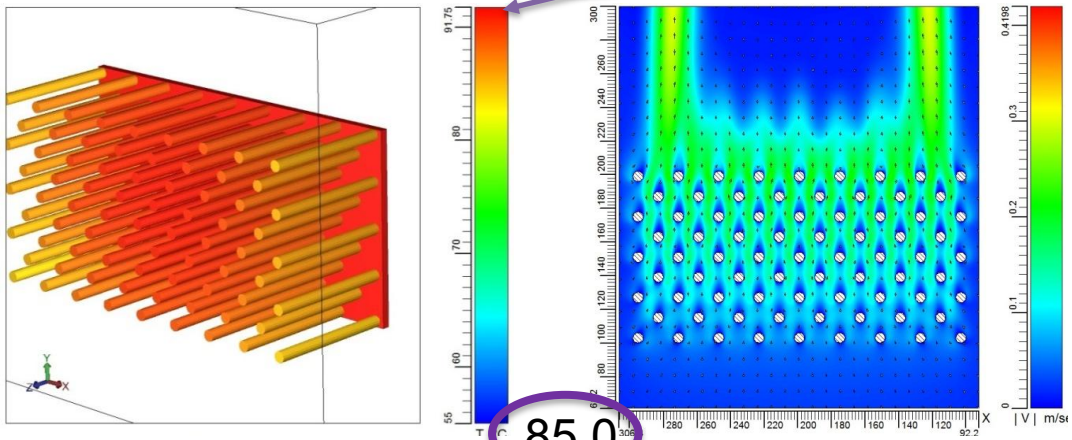
Haet sink Opinations

Free Convection Example

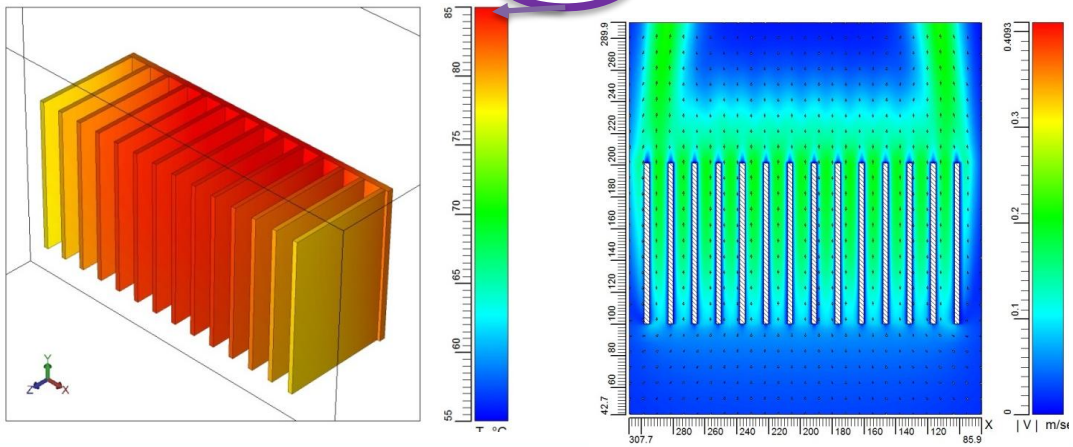


Base plate:
200x100x4 mm

Pins



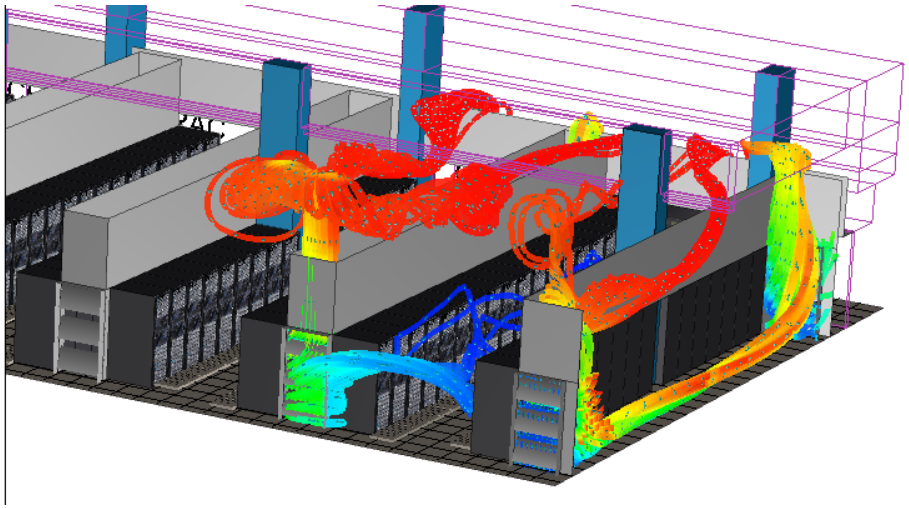
Fins



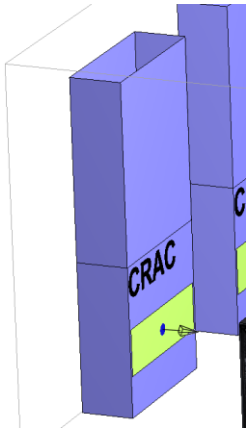
Data Center Booming

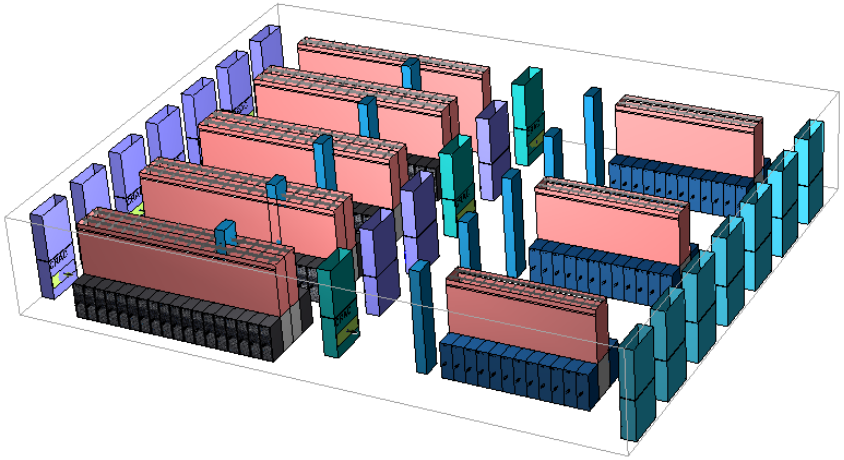
Liquid Cooling Influences

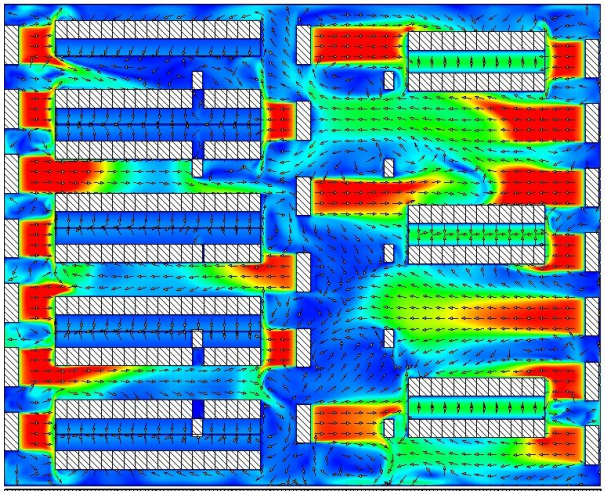
- The AI leads to increasing in computing power and the adopting of liquid cooling due to the higher thermal density and air-cooling limitation, but at typical modern hybrid data canter, the cooling is roughly 80% liquid/20% air , and CFD simulation is still needed for the air-cooling part.

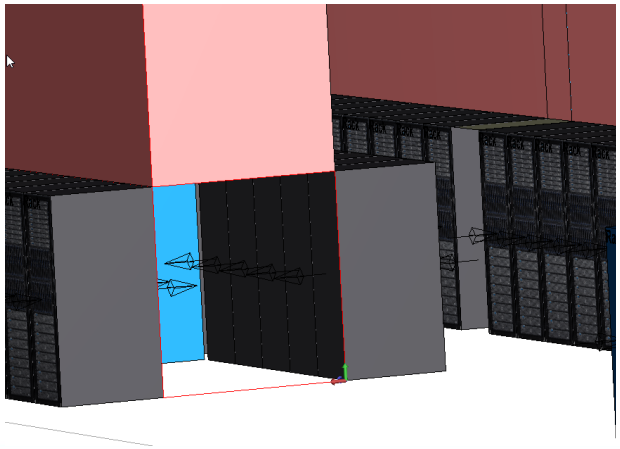


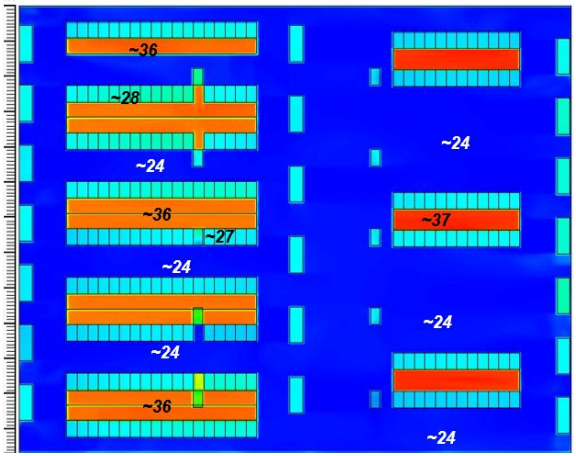
Data Center Structure And Simulations

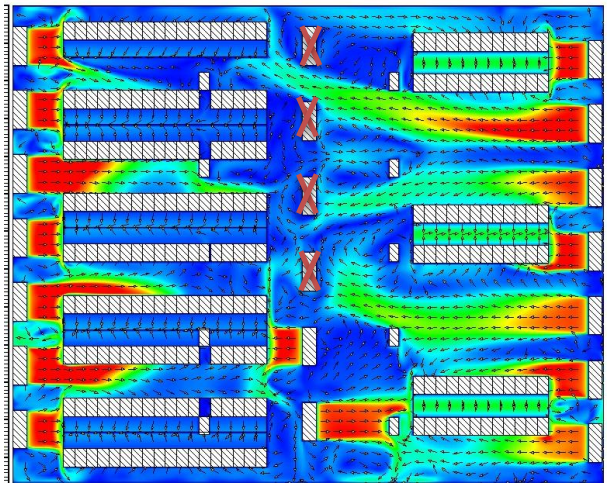






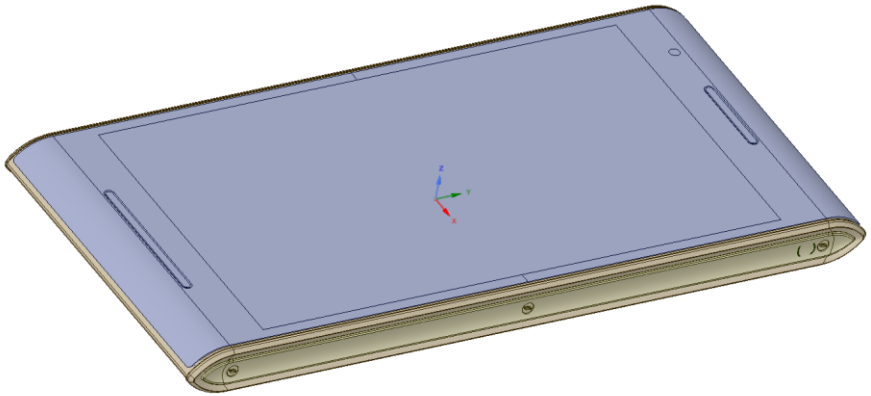


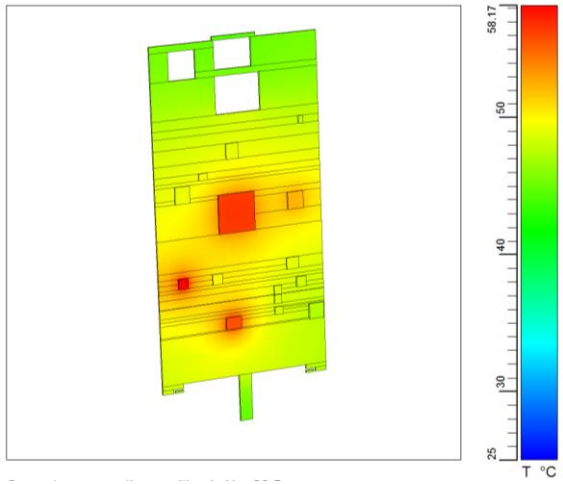




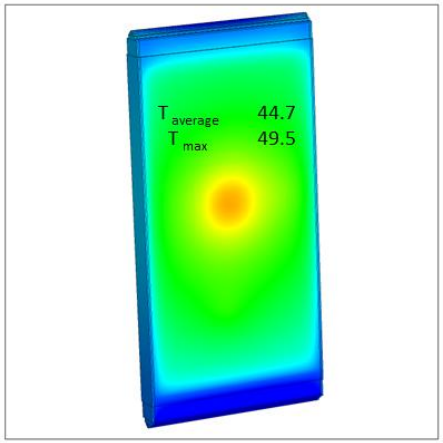
Mobil Phone

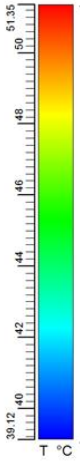
Mechanics Model and Results (Temperatures)





Front side CTS = 0.8





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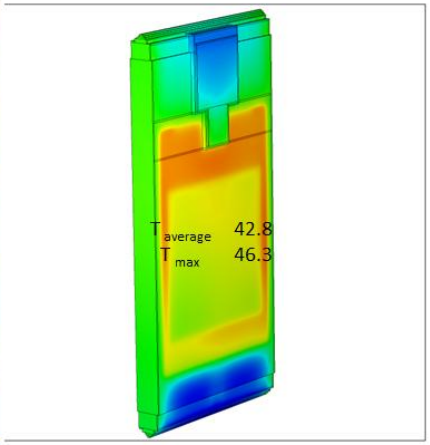

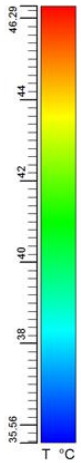

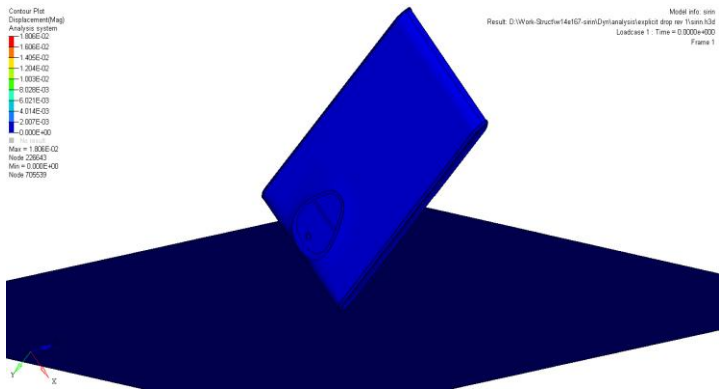

Thanks
Questions ?