Leveraging Formal Verification to Boost Chip Development Process

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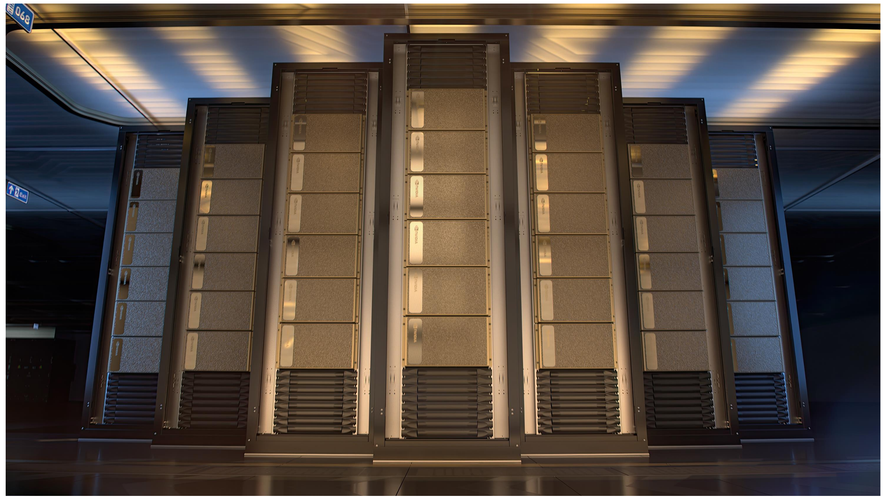
What is formal verification

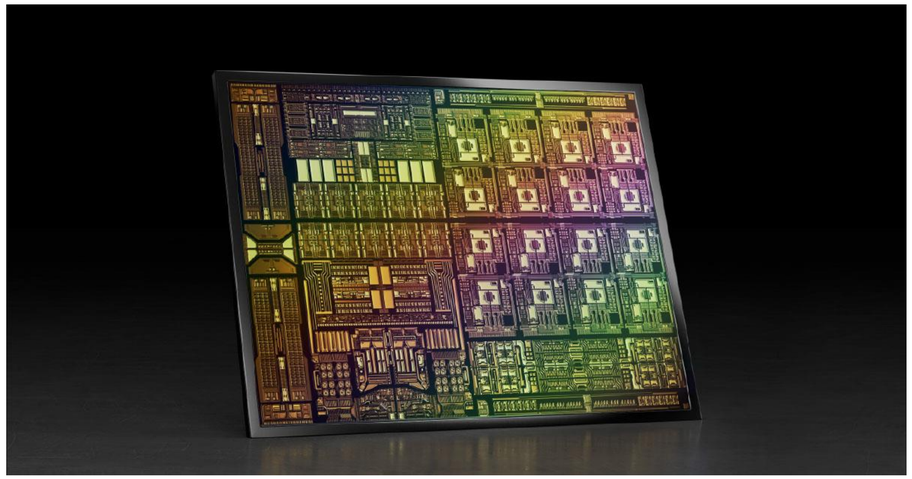
- Formal Verification is the act of Proving the correctness of a design using formal methods of mathematics
- Formal can prove that an expression is always true. This expression is the outcome of a logical design and defined as an assertion



Chip design main goals

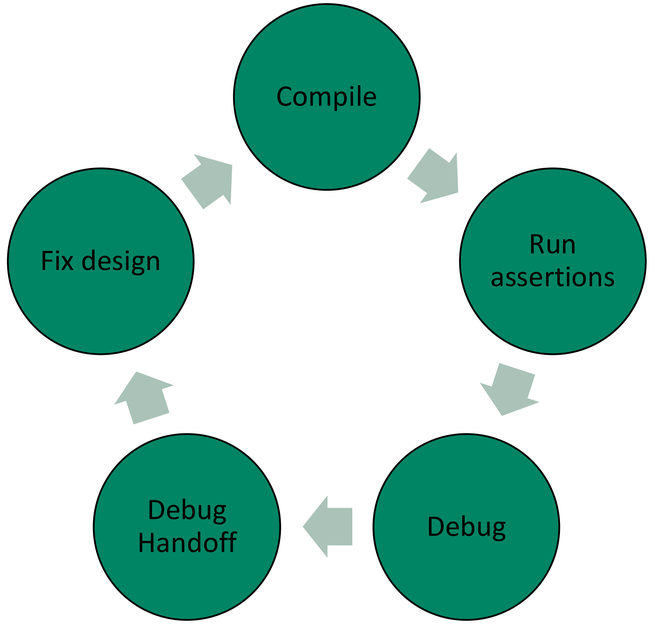
- TO on time
- Zero bugs delivery
- High efficiency

- **Formal Verification is a mean for achieving these goals**



Formal Verification Objectives

- Quality
  - Clean of bugs
  - Achieving Robust design
- Fast convergence
  - Fast ramp up
  - Easy debug
  - High return on investment.
- Emphasis where DV is ineffective
  - Possibility to run only FV.
- Double check with DV on complex and critical areas.



Nvidia Networking FV Team

- We apply Formal Verification and understand its great value from Mellanox early days
- During the years we professionalized on how to make out the most from this powerful tool
- Nvidia networking Formal Verification team:
  - Managed as central group
  - Integral part of the chip design group
  - Dedicated team for each product (NIC, Switch, CPU, IP’s)
  - We insist on getting the best technology to our engineers.
    - We use industry standard tools
    - We develop an in-house Formal verification platform and engines

Formal Verification during micro arch stage

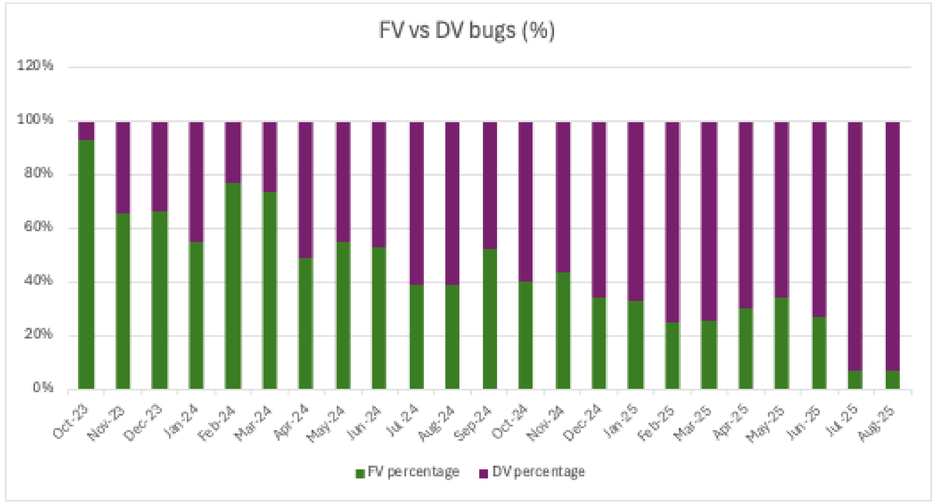
- We involve Formal expert during the micro architectural stage of a project.
  - Tune u-arch definition for ensuring efficiency later on
  - Identification of FV models and the HR needed for each task
  - Parameterization of the DUT
- Identification & parameterization stages should be reviewed by expert Formal engineer to have high efficiency.
- We collaborate with our design engineers to guide them how to code their design best for FV

Formal management

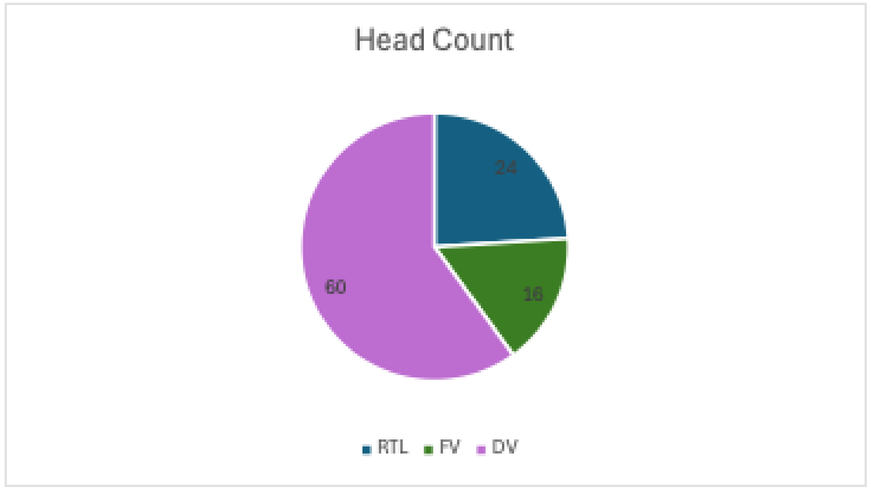
- Optimal HR assignments
- Every line of code in the project has formal ownership
  - Keep focusing FV to the most efficient areas
- Formal is part of the project KPIs
  - FV MAS
  - Milestones checklists
  - Signoff
- Formal group is constantly challenged by management
- Project managers/designers are evaluated also on the FV quality in their domain
- Formal managers are an integral part of the steering group of the project

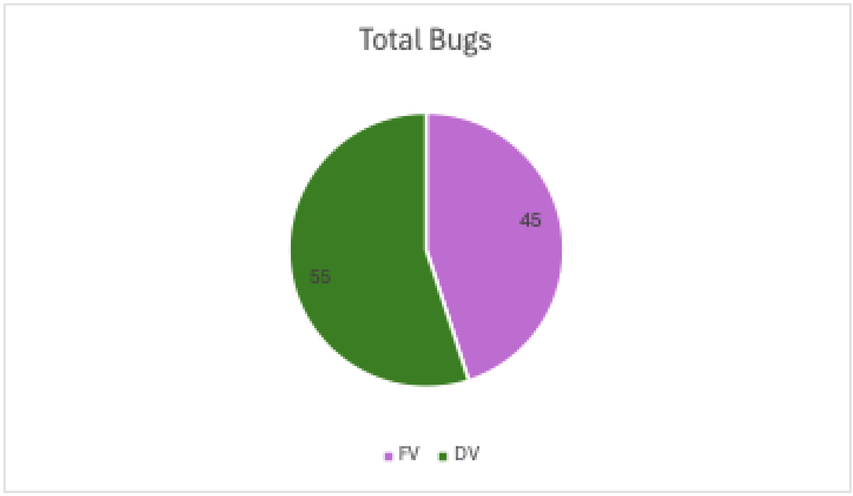
Formal Effectiveness in Nvidia Chip Design

- FV bugs per engineer are very effective
- Formal ramp up is very fast, first bugs can be found in hours
- FV bugs found per project rang from 30%->51%



- **Chip design project managers are demanding more and more Formal**



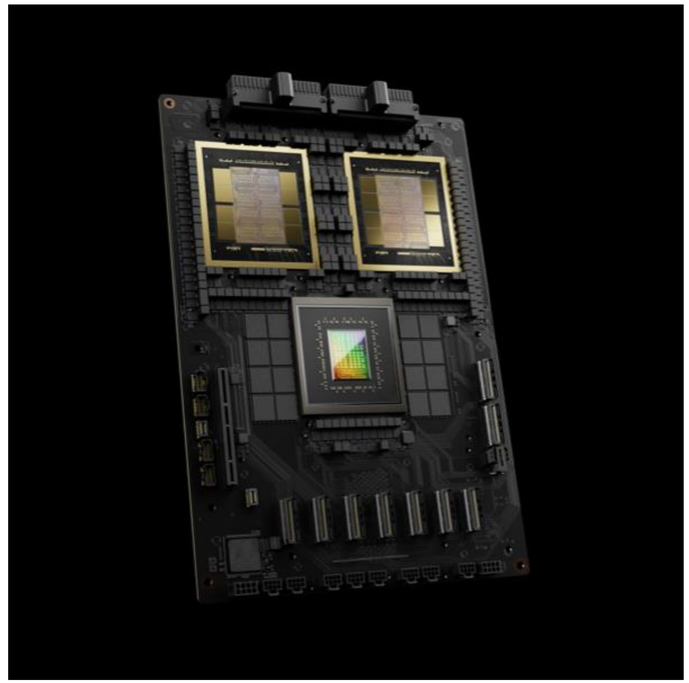


Summery

- Micro-arch definition involvement by expert FV owner
- Assignments of Formal owners to specific units (taking under consideration complexity, ROI and HR)
- MAS stage: Formal Verification unit owner presents FV MAS.
- Continues verification work on the units, according to well defined priorities .
- FV Signoff: Formal Verification Checklists are done by FV owners (in parallel to design and DV Checklists)

Formal Verification roles and ownerships in a running project

- Formal Verification project manager
- Formal Verification cluster manager
- Formal Verification unit owner
- On every piece of code there’s a FV owner in charge to decide if/how to FV it



Formal <-> Dynamic relationship during a project

- FV and DV work at a specific unit have good correlation in order to give the full verification solution
  - Each design block contains multiple features with different ROIs
  - Formal will check some of the features to zero bug level:
    - a-synchronic interfaces (interface with free sequence between them), like arbiter
    - Inputs with a lots of options (like parser)
    - Deadlocks, credits
  - There are features that can’t get to 100% cover by Formal with good ROI vs DV
    - Blocks with system orientation (most bugs will be found in integration)
- Formal can cover blocks and units up to 100%
- Formal verification should start before DV to assure efficiency
- Signoff features that passed Formal are 100% clean of bugs